Study and Implementation of BIST Architecture

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ABSTRACT

A Built in self-test technique forge a category of algorithms that endue the potencies of performing at speed testing with elevated fault distribution. Main motive of the paper is to make BIST architecture by using a test pattern generator (TPG) which links a linear feedback shift register (LFSR) with several applications [1]. Design for testability (DFT) schemes are used for calibrating of circuits like as built in self-test architectures (BIST). Safety in devolution of codes is a huge dare in these days as the competence of transcribing of data make little day by day [3]. BIST architectures are typically divided into on and off-line. Autonomous architectures work in the regular or essay (test) mode. The input signals originated by the test generator module in the test mode, are embed to the input of the tested circuit (CUT), and the outcomes of the Response Verifier (RV). Using ML (maximal length) LFSR, many drawbacks like BIST architecture introduce more switching activities in the circuit under test during test than that during ordinary operation because of the intense power dissipation and outcomes in delay penalty into the design, which are responsible for imbalance of data as long as relocating from one to different location, hence safe transferring , may not be easier, to overcome with these problems we use BIST (Built in Self-test) circuit, with BIST (Built in Self- test) circuit, power dissipation can be reduced , need little area.

Keywords: Built in Self-Test, Test Pattern Generator, Multiple Input Signature Register, Circuit Under Test , Linear Feedback Shift Register.

I INTRODUCTION

Testing is nothing but the application to check the circuit response, "Application which checks the actual circuit response with correct circuit response". The Process of use up a product and examine its resulting response to check if only faults are proposed during the manufacturing or operation phase [1].

The process of use up a product and examine its resulting response to check if only it functions correctly [2]. Process of determining if only a product functions correctly General purpose testers are normally applied for this objective. But they are so expensive and this is not only the problem there are some cases with this:

Time: The whole time to originate the assay (test) stances, the time period to apply the assay (test) stances, and the time term of computation are increasingly too huge [4].

Volume: There are very large numbers of test patterns to be managed proficiently by the tester hardware [4].
To overcome with these problems we use BIST (Built in self-Test) technique. "Built -in self-Test; this is the strength of a circuit (chip, system, board, product) to test itself". it is a conjunction of the notion of built in test and self-test. By using the concept of BIST, there is a great reduction in the testing time. BIST techniques are divided in many types, but some widely used manners of Built in self-test are:

In On-line BIST, in this type of testing, testing exist during normal functional operating conditions and at this condition where functional operation is locked out, the circuit under test not to be located into a test mode [2]. In Off-line BIST when the system is not going through with its normal functions at the condition only it deals with testing a system. At this phase board, system & chips can be test. This type of testing is appropriate also at the manufacturing, field & operational level. Most of the time Off-line testing ceases using (On chip & board) TPG and ORA etc. it can't find defects in virtual time that is when they first become.

It is proved that Built in self-test is one of the most economical and generally used for testing solutions & these reasons:

- No need Exterior equipment for testing
- Reduced advancement efforts
- Testing is able in On-line or Off-line

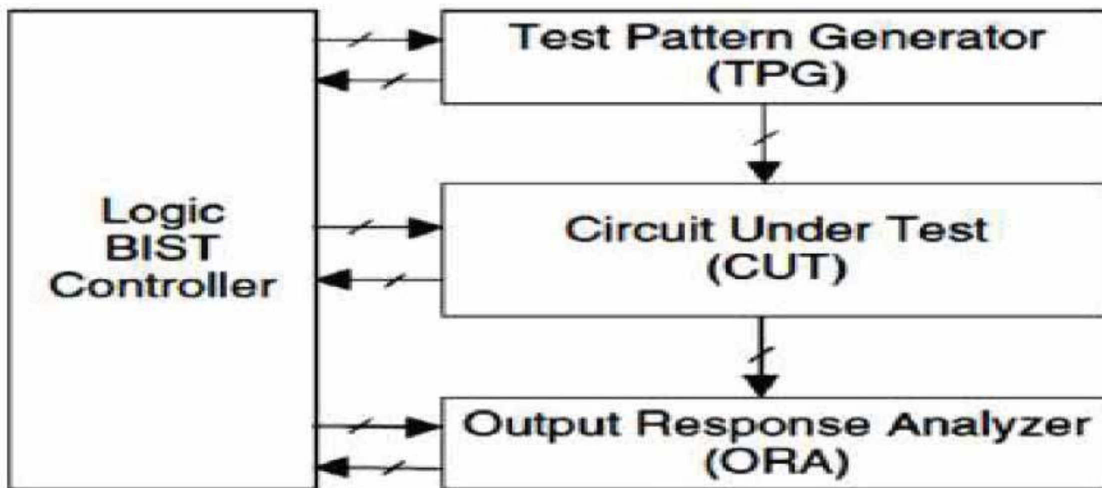

Fig No.1 Basic BIST Architecture with BIST controller and three Blocks

II LITERATURE REVIEW

(a) Background and Motivation: The involution of circuits is increasing day by day, so testing the circuit from i/p, o/p pads becomes laborious and time consuming. Hence there is the necessity to reduce the complexity of testing. For this purpose BIST is developed. Built in Self-Test or BIST, is the system of working, where extra hardware (H/W) and software (S/W) characteristics into integrated circuits to permit to execute self-testing (test itself), that is, verifying of their personal manipulation (functionally, parametrically, or both) using their personal circuits, this thing decreases dependency on an ATE (external automated test equipment).

(b) BIST (Built-in Self-Test): Built-in self-test, "The elementary consideration of BIST, in its dire unpretentious form, means the impulsive to cam a modus circuit which can test itself and apprize if only it is 'nice' or 'nasty'…" [5].

By dealing the notion of BIST, there is a gigantic scarcity in the calibrate time. The built in test equipment (BITE) signifies to the hardware and/or software comprised into a unit to terminate DFT (Design-for-Testability) or BIST ability.

"BIST ordain by dint of test at pertinent worth. Because of BIST, chip overhead be able to abbreviate by a prudent elect of implementation techniques".

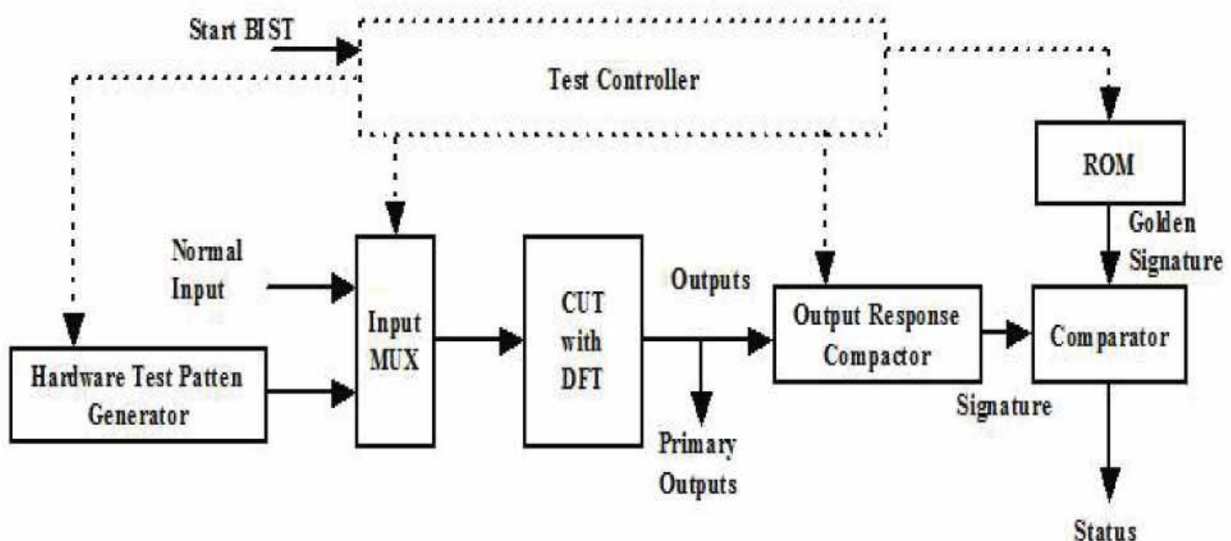

Fig. 2 Typical BIST Architecture

(c) **Types and Technique of BIST:** BIST techniques are divided in many types, but some widely used manners of Built in self-test are:

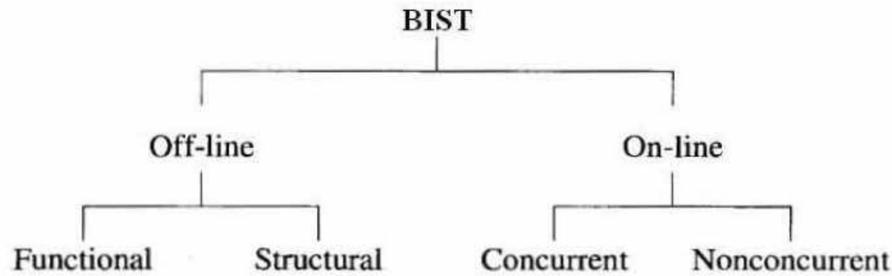

Fig No. 3 Types of BIST

(d) **Merits and Demerits of BIST (Built in Self-test):** Special test structures can be affined among the chips because fault coverage is preferable, If the BIST can be textured to test more structures in parallel, then test time may be shorter. BIST is easier customer endorsement. BIST have potency to perform tests outside the production electrical testing environment. It allows the consumers themselves to test the chips prior to mounting or even after these are in the application boards [4].

BIST have some drawbacks also like Area overhead, Performance penalties, Additional formation time & effort, Additional peril to Scarcity of orthogonal testing etc.

(e) **Working Procedure of BIST Architecture:** The BIST architecture is the aggregate of three hardware fragments. It's necessity the addition of these three hardware fragments to a digital circuit. It is a design-for-testability (DFT) technique which corporally instituted the calibrate functions with the circuit under test (CUT) [2].

(i) Test Pattern Generator (TPG)
(ii) Output Response Analyzer (ORA)
(iii) Test Controller (TC)

Task of the test pattern generator is originate test patterns for Circuit under Test, then a Response analyzer is merely as an LFSR which is consumed as a signature analyzer , it handles and analyze the responds to apprize accuracy of the CUT, then test controller activate the test and examine the responds. In general way many test related fun. can be verified by dent of a TCU.

(f) **TPG (Test Pattern Generator):** TPG totally depends upon the blemish in the test vector that is evolved for the purpose of CUT. The function of TPG is to originate the test vectors and definitive in CUT correct sequence [2]. The hierarchy is stored in ROM with immobile test patterns, linear feedback shift register etc. The LFSR's outputs are time shifted & repeatable; this decreases the impactness of the fault detection because they become corefered.

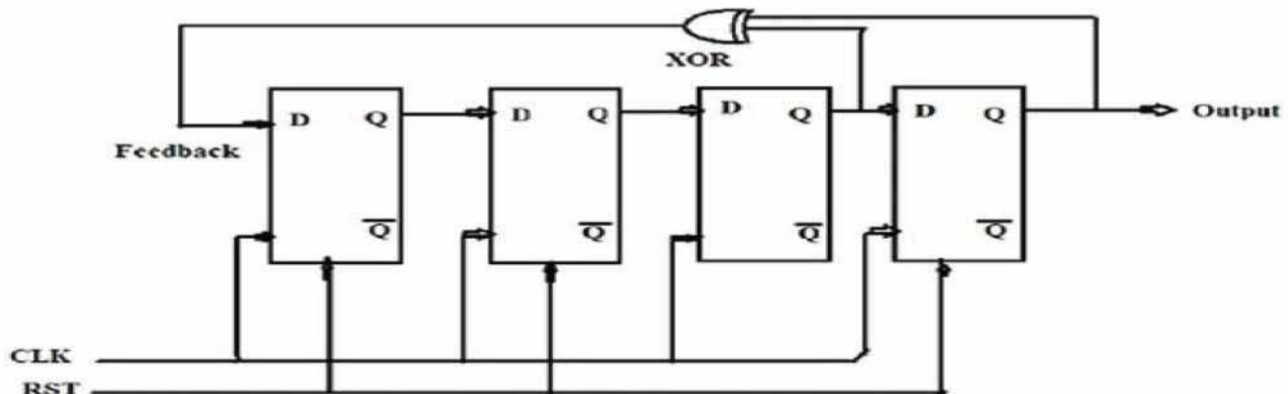

Fig. 4 4 bit LFSR (Internal Feedback)

(g) **CUT (Circuit under Test):** The CUT acquires its inputs by means of another module and executes the function for which it was conformation. Among test mode, a test pattern generator (TPG) circuit enforces a hierarchy of test sampler to the CUT, and the responses of the test are evaluated by an output response analyzer.

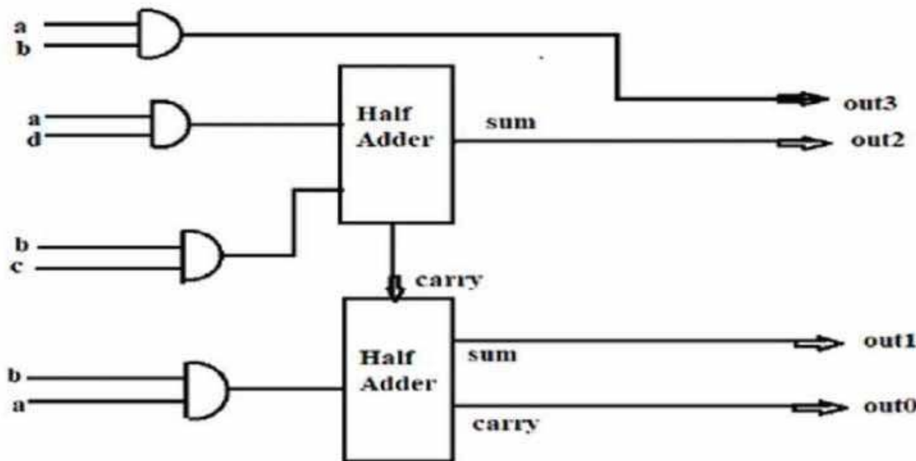

Fig. 5 CUT (Circuit under Test) with 4 outputs, to reduce power dissipation use 4 bit CUT

(h) ORA (Output Response Analyzer): The test vector importance is to examine the response of the system and system decision being inaccurate or fault-free [9]. The system output respond of the CUT is compared with the responses which are fault free by the ORA. The ORA compress the response of the o/p cams with single pass/lapse clue from the CUT [10].

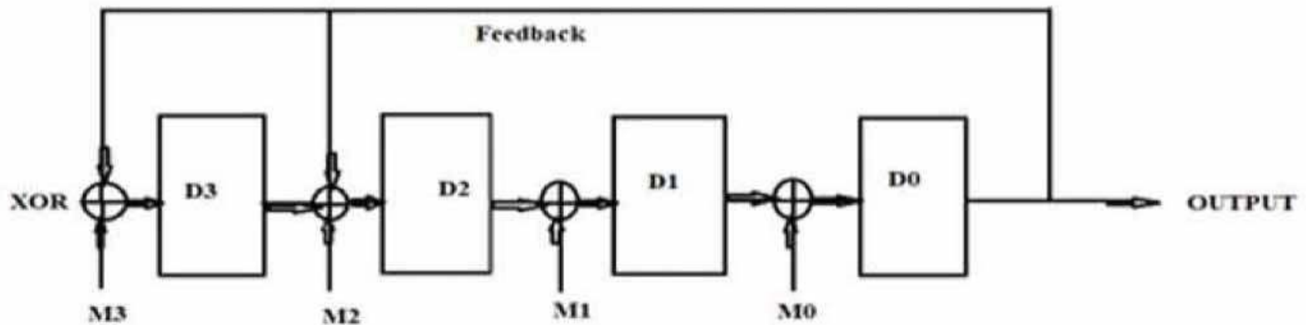

Fig. 6 MISR (Internal Feedback) with 4 parallel inputs

(i) Test Controller: The BIST controller cherishes the swaps to execute the test. The test can communicate with second tested controller for system integrity. The external interface of the test controller contains isolated input and output signal which are applied to initiate the self-test sequences. CUT is placed in the test mode by the Test Controller and it activates the i/p isolation circuitry and allows the TPG. By the use of the test controller implementation, it may be amenable for providing root values to the TPG. Then the outputs respond interacted by the test controller to ensure the appropriate signals compared [10].

III SIMULATION RESULTS

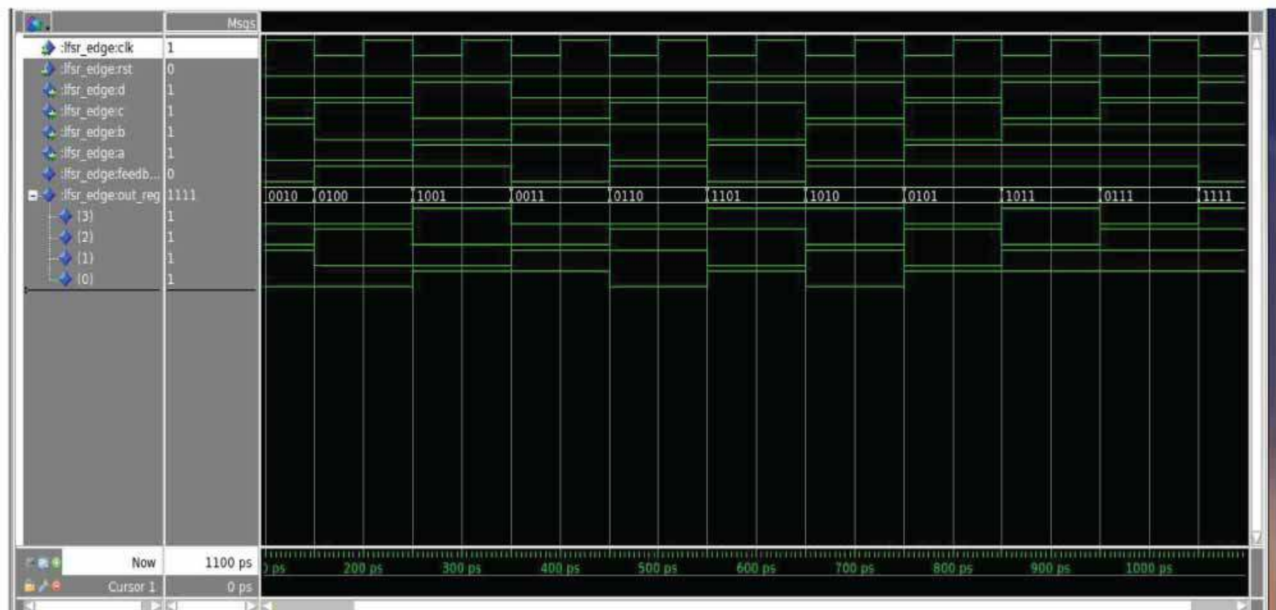

Fig. 7 Simulation Result of 4 Bit LFSR (Linear Feedback Shift Register) generates random & repeatable patterns.

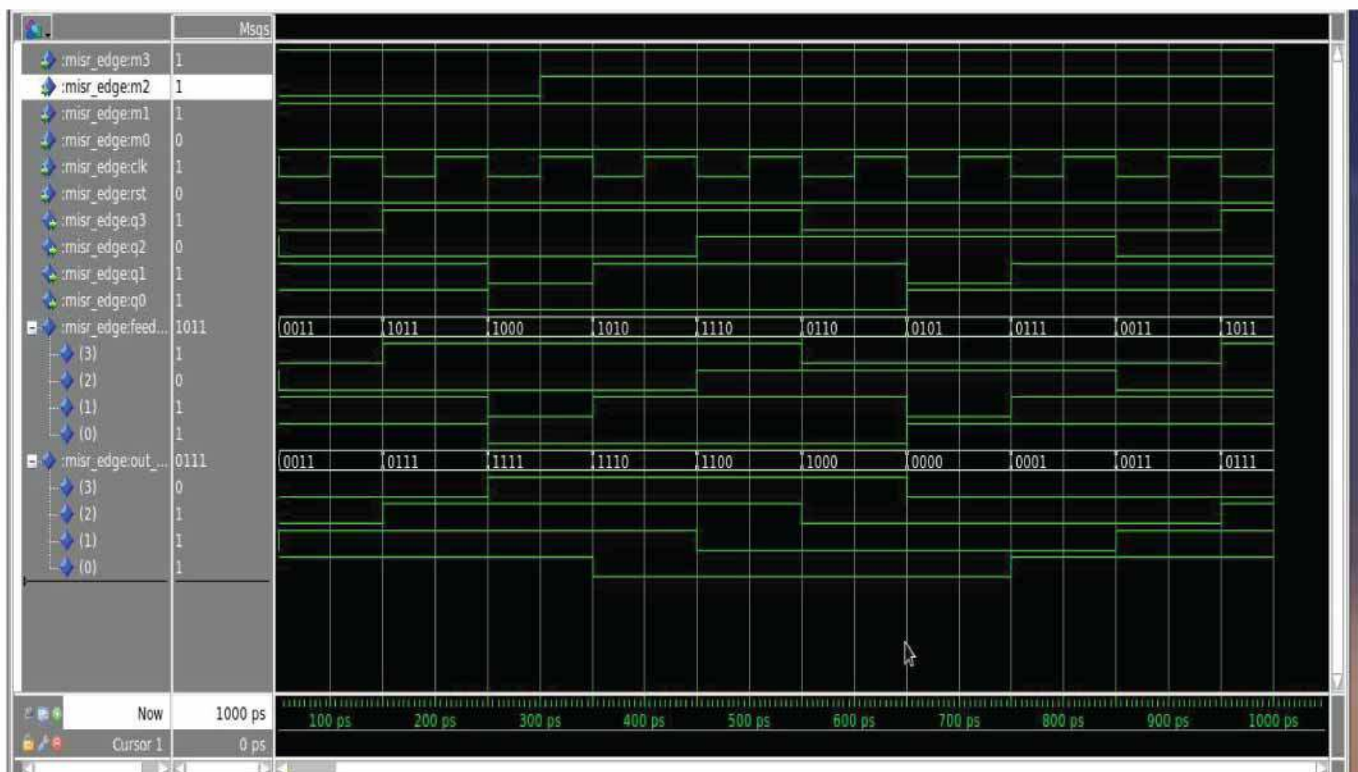

Fig. 8 Simulation Result of 4 Bit MISR (Multiple Input Signature Register) with parallel inputs.

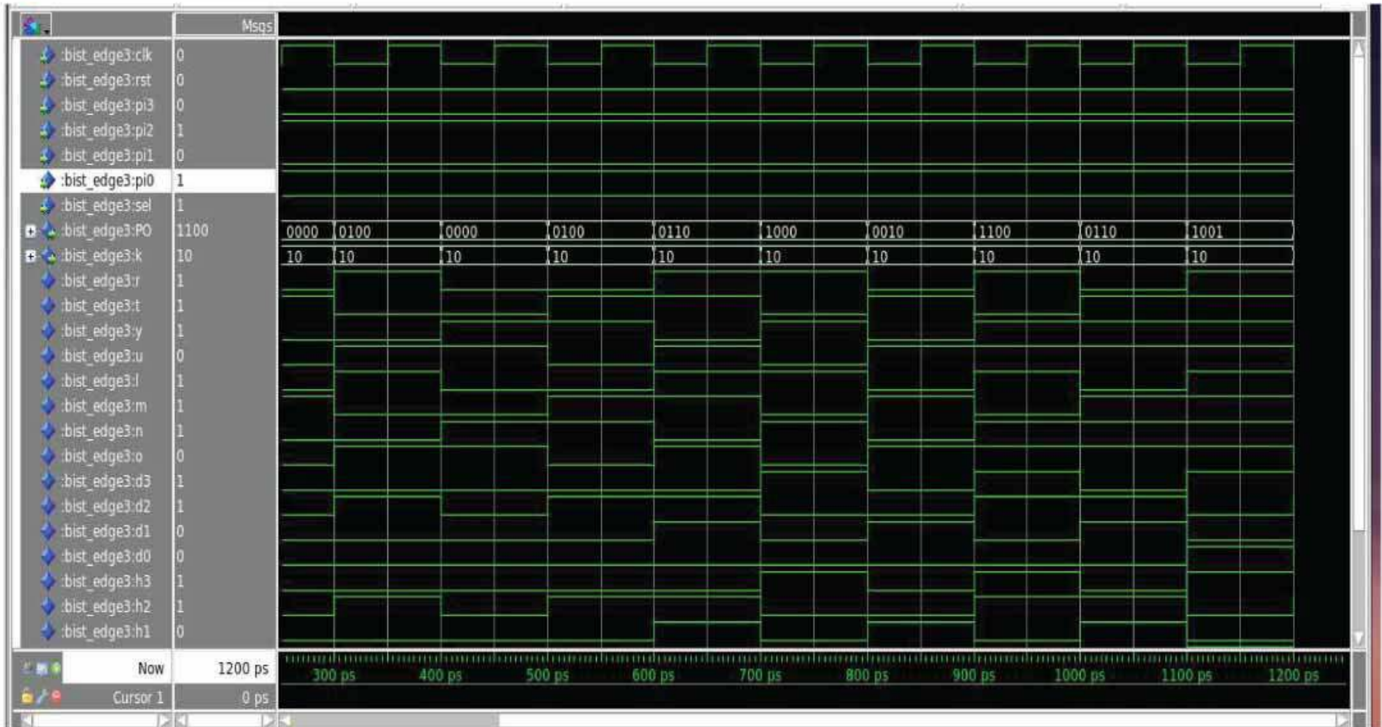

Fig. 9 BIST Simulation (pass indication)

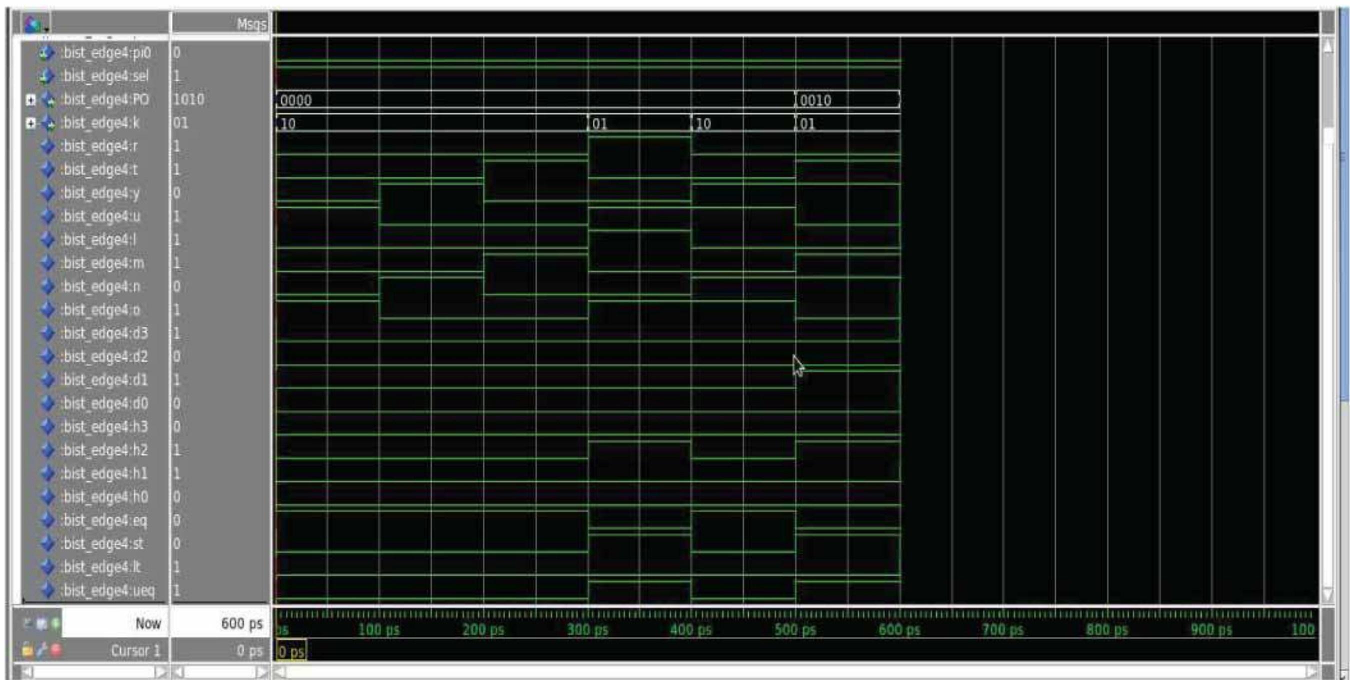

Fig. 10 BIST Simulation (Fail Indication)

IV CONCLUSION

This paper perfectly assigns BIST architecture. Built in self-test has been evolved as an appropriative alternative testing strategy, here to reduce power dissipation, delay in results and reduce switching activity in the circuit and make capable the circuit to test itself, we use BIST architecture. In this paper we implemented architecture of BIST circuit.

Dependence on the external automated test equipment (ATE) makes little by BIST (Built in self-test) circuit. There is no straight or perpendicular relations of complicated circuits to external pins, BIST is the best option to the testing of these types of circuits, these type of memories applied initially by the devices. Even in the coming future, the testers will not be of any use for the fastest chips there self-testing will be required.

BIST will be of greater deployment in variety of applications. BIST is now an alternative solution for the testing device. It can be used in wireless communication. it is used in real products like semiconductors and computer industrial.

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