Design and Implementation of 12 bit Pipeline Analog to Digital Converter

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ABSTRACT
The Power dissipation and chip area of analog and mixed-signal circuits emerged has as a critical design constriction in today' s VLSI design systems .This paper presents a multilevel design optimization for reducing the power dissipation and high sampling rates of a pipelined analog-to-digital converter. A 12 b 75-Msample/s analog-to-digital converter has been fabricated in a0.18-um CMOS technology. The converter uses pipelined seven stages and implements 2 bit per stage architecture. It is a fully differential analog circuit with a full-scale sinusoidal input at 20 MHz. It dissipates 3.5mW.

Key Words: - Operational Amplifier, Pipe Line ADC, S/H Circuit, Comparator.

I INTRODUCTION

Enabled by the long-lasting destructive scaling of integrated circuit technology, digital signal processing (DSP) and computing have developed into the main progress drivers in modem electronic circuits. With decreasing number of transistors and transistor dimensions, binary totaling are performed at lower energy levels, low power dissipation and higher speed, resulting in an increasing number of highly sophisticated architectures and algorithms that can be capably implemented using integrated digital electronic circuits. Most essentially, the concurrent requirement of high speed and low distortion and low noise and less chip size in the processing of analog signals often translates into poor power effectiveness and limited accuracy. In addition to decreasing supply voltages and reduced intrinsic transistor gain in modern electronics technologies make the design of highly linear, high energetic range analog edifice of blocks an increasingly challenging role [1].

As an outcome of these tendencies, manufacturing lean towards a system separation with a minimum number of virtually necessary analog parts. Amongst them is the Analog-to-Digital Converter (ADC), which is required to interface digital signal processors to "real life" signals such as radio, satellite, system image and speech waveforms. The exploration for the most part concerned with improving the speed and power efficiency and accuracy of analog to digital converters. In particular, we explored the prospect to overcome analog circuit

In CMOS technology, an easy advance is to use Flash ADC [3]. CMOS flash ADC's with array averaging is reported to realize a 1.3 G samples/s alteration rate. However the complexity and power dissipation of the flash ADC grows exponentially as resolution increases because the number of comparators increases by 2n (where n is the resolution of flash adc). This makes flash ADCs inappropriate for resolutions greater than 8 bits because they consume large area and high power dissipation as well asc. Many high speed ADC architectures have been reported to try and conquer the problems of flash ADCs. Sub-ranging, pipeline and folding & interpolating architectures are illustrations of such efforts and have been successful in many video/image processing and communications , modem medical imaging applications [4],[5]

The Pipeline ADC implemented in this approach is a dynamic approach that combines the ease of a flash with the residue type operation for pipeline implementation. Many novel ideas have been implemented to improve the architecture such as forefront and backdrop calibration [6],[7],[8].

II PIPELINE ADC ARCHITECTURE

Pipeline ADC architecture radically reduces the number of comparators required to realize an n-bit conversion per stage and, hence, increases sampling frequency and requires the analog bandwidth and maximum sample rate of the converter. They also consume considerably less power, less area high throughput thereby reducing linearity problems associated with thermal gradients. This type of architecture proposes the most resolution at high speeds of any accessible ADC architectures. A pipelined analog to digital converter is a good example of a pipelined signal processor. One example of a pipelined analog to digital converter is a pipelined sub ranging analog to digital converter. In a sub-ranging ADC, the conversion operation is alienated into a number of steps. During each stage of the conversion, a certain number of bits of the digital output are resolved. The most significant bits are resolved in the first step, and the least significant bits are resolved in the last stage the pipeline ADC architecture as shown in Figure 1 operates on sample-and-hold (S/H) in every stage to Multi increase the throughput. Each stage consists of an S/H, an N-bit flash ADC, a renewal DAC, a subtractor, and a residue amplifier. Pipelined converters are more frequently used to realize high

conversion rates per stage since they provide effective signal bandwidths equal of 10-100 MHz (sample rates of 20-200 MHz). The conversion method is similar to that of sub-ranging conversion in each bit stage.

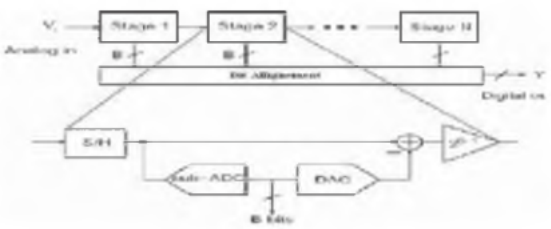

Fig 1. Block diagram of a pipelined ADC

This is mathematically described as-

$Vi = 2 * Vi\text{-}1 - bi\text{-}1 * Vref$ ----------(1)

Where bi-1 is given by

bi-1 = +1 if Vi-1 > 0

-1 if Vi-1 < 0

III CIRCUIT IMPLEMENTATION

Each stage consist on this schematic shown in fig 2

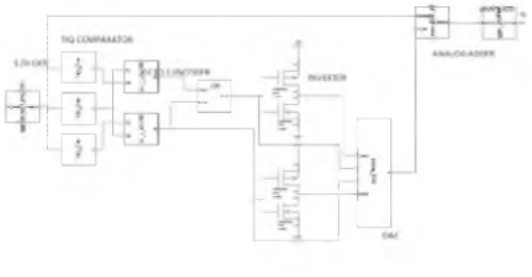

Fig. 2 Schematic of Single Stage of Pipeline ADC

For the implementation of each stage of pipeline ADC the need of components are

(a) Sample and Hold.
(b) TIQ Comparator.
(c) 2-bit DAC.
(d) gain Amplifier of 4.
(e) tc to bc encoder
(f) Operational amplifier
(g) D flip-flop

IV SAMPLE & HOLD CIRCUIT

The basic elements of a Sample & Hold circuit are a storage element and a switch.

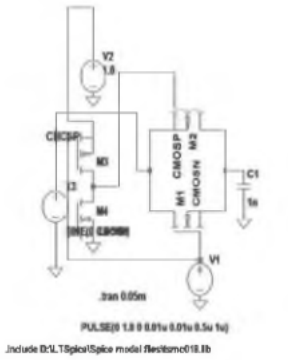

Fig. 3 Schematic of S/ H Circuit

Sample-and-hold circuitry is essential for ADC front-end circuits to permit the ADC to track and then hold the inmost bound signal. (See [8] for argument of sample and hold circuitry.) Once the signal has been tracked, the ADC pitch a switch to disconnect the input signal from the front end it then holds that input signal level long Enough for the ADC to entire its conversion cycle

V DESIGN OF COMPARATOR

Implemented flash ADC features the Threshold Inverter Quantization (TIQ) technique for high speed and low power ADC using typical CMOS technology.

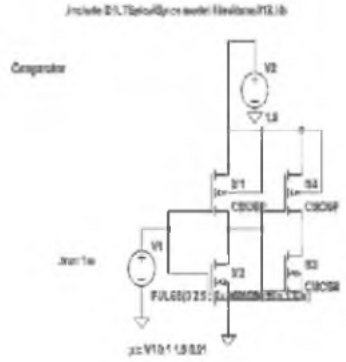

Fig. 4 Schematic of Comparator

Fig. 4 shows the circuit diagram of the TIQ comparator. The use of cascading inverters the same as a voltage comparator is the cause for the technique's name. The voltage comparators compare the input voltage with internal reference voltages, which are decided by the transistor sizes of the inverters. We have supposed that both transistors are in the active region, the gate oxide thickness (Cox) for both transistors will be same, and the lengths of both transistors (Lp and Ln) are also the same fig.

Escalating equation

$$V_t = \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}}(V_{dd} - V_{tp}) + V_{tn}}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}}$$

wherever, μp and μn are the electron and hole mobility.

VI DESIGN OF TWO BIT DAC

Nearby various arrangements that can be utilized to design digital to analog converter (DAC) like resistor ladder (voltage divider architecture), charge division principle, current division architecture and many additional, but all of this employ lot of components and are complex in nature. Therefore to digital CMOS technology, multiplexer logic has been utilized to behave like DAC, seeing as the purpose of DAC is to provide an analog voltage analogous to digital bits, as shown in fig 3

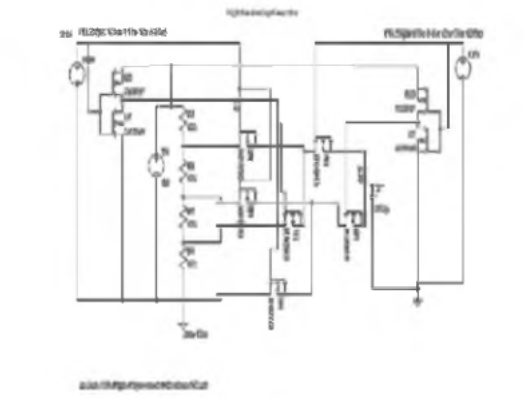

Fig. 5 Schematic of 2-Bit DAC

VII DESIGN OF D FLIP-FLOP

Flip-flops are the most traditional storage elements used to realize synchronous logic circuits. . It is one of the necessary elements in the pipeline ADC, the major point to elevate here is that, it is used as delay element which will synchronize the bits of the all stages, by configuring the flip-flop as unreliable length shift register. it will synchronize the output of pipeline ADC. For example for 7 bit pipeline ADC, first stage has 7 bit shift register, in the later stage it will be of length 6 and decrementing to 1 in the last stage. The additional use of this flip-flop is in the end of alteration signal generation

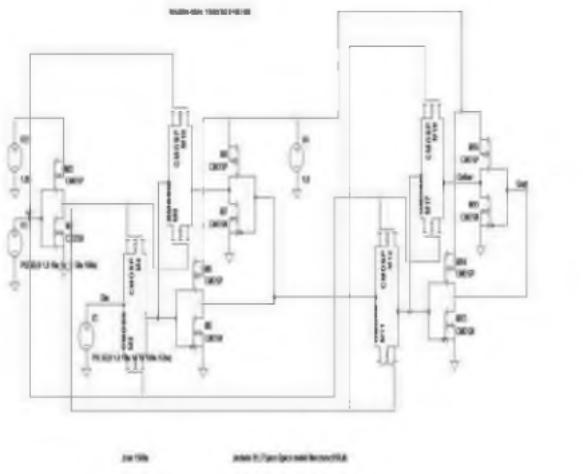

Fig. 6 Schematic of D-Flip-Flop

in which it is build up as counter which will set up counting when the ADC get start of conversion signal and will be stopped up after counting seven clock cycles.

VIII TC TO BC ENCODER

The encoder converts the 01 code in to the 1 code in two ladder. The 01 code is changed to the 1-out-of-n code, through the '01' generators. This code is then converted to binary code. Shows in fig a single cell optimized '01' generator circuit by signifies of only four transistors, only if full swing output in a small design area.

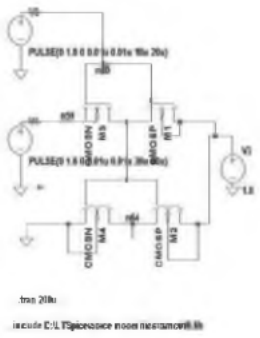

Fig. 7 Schematic of TC to BC Encoder

IX DESIGN OF INVERTING GAIN AMPLIFIER

Each stage of pipeline ADC stage has one gain block, whose gain depends on the number of output bits per stage. Thus the OPAMP has to be configured in closed loop style

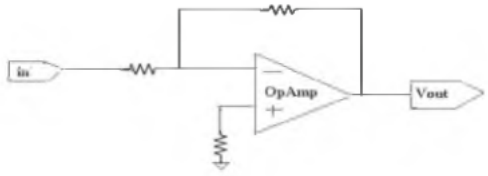

Fig. 8 Inverting Gain Amplifier

X DESIGN OF TWO STAGE OPAMP

Operational Amplifiers are the vertebrae for many analog circuit designs. The speed and accuracy of these circuits depends on the bandwidth and DC gain of the Op-amp, the realization of a CMOS OPAMPs so as to combines a significant dc gain with higher unity gain frequency has been a the majority of difficult problem. There have been several circuits proposed to evaluate this problem. The purpose of the design methodology in this paper is to propose accurate equations the following specification have been used for design of the two stage OPAMP

Vdd = Vss = ±1.25
Av = 5000 V/V = 73.97 dB
GBW ≥ 100 MHz
Slew Rate ≥ 30 V/µs;
ICMR = ±0.8 V
C_L = 5pF
For 60^0 phase Margin, C_C>0.22 C_L
C_C=1.5pF

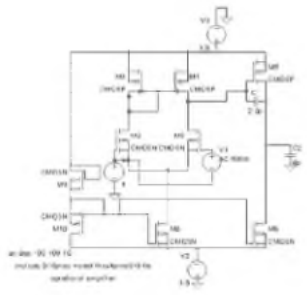

Fig. 9 Schematic of Two Stages Operational Amplifier

XI SIMULATION RESULTS

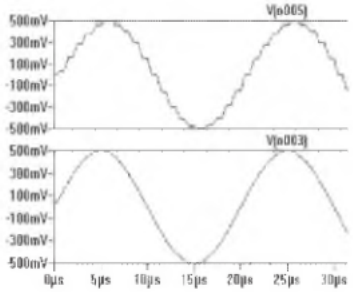

Fig. 10 Transient Result of Sample & Hold Circuit

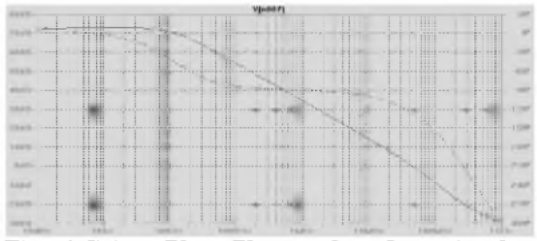

Fig. 11 Gain & Phase Plot Result of Operational Amplifier

Gain=75.94dB,Unity Gain Frequency=100MHz
Slew Rate= 200v/us
CMRR= 79.397dB

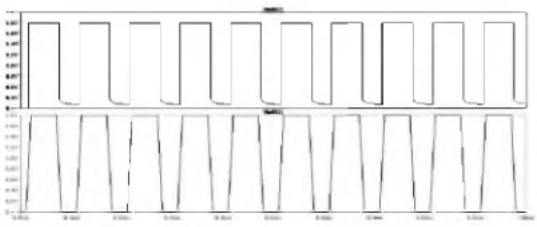

Fig .12 Transient Analysis of Comparator

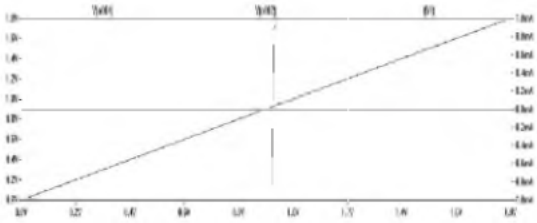

Fig. 13 DC-Sweep Characteristic of Comparator

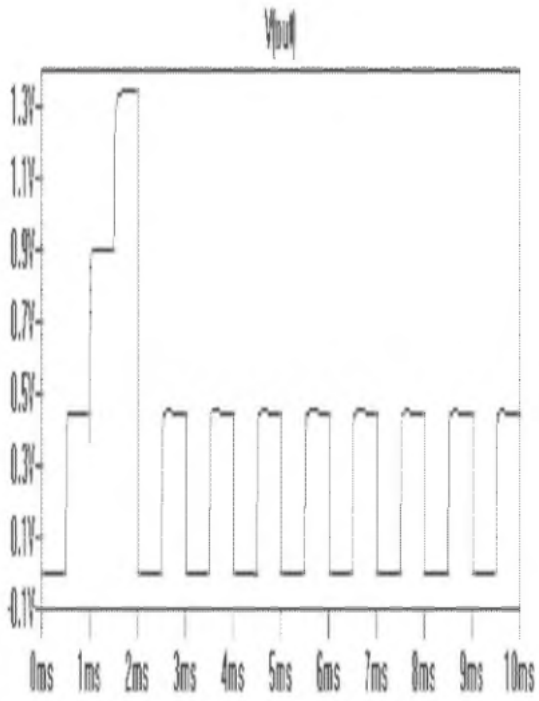

Fig. 14 Transient Results Of DAC

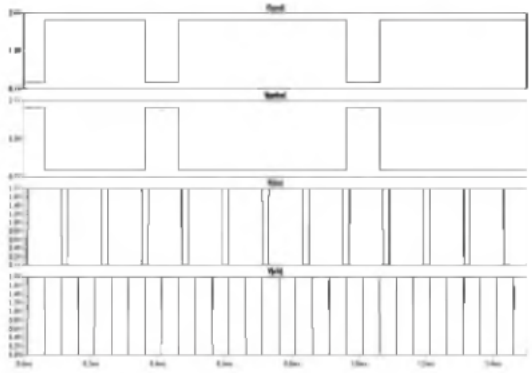

Fig. 15 Transient Result of D-Flip-flop

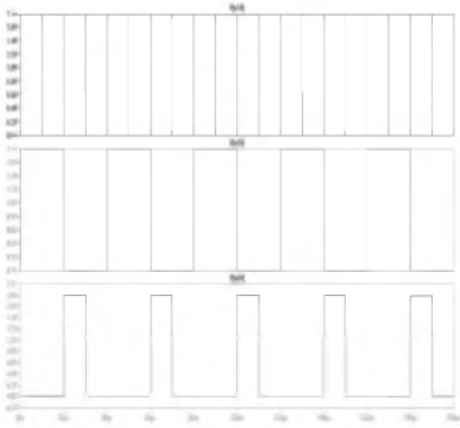

Fig. 16 Transient result of TC- TO -BC Encoder

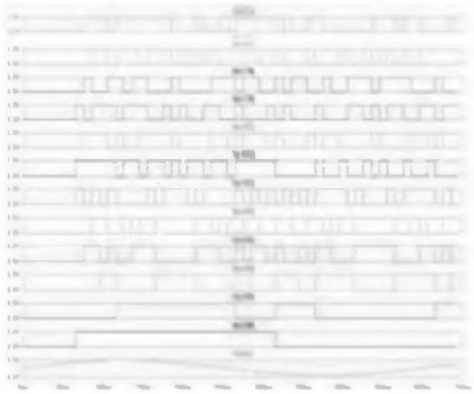

Fig. 17 the plot of 12-bit pipeline ADC with sinusoidal input

XII CONCLUSION

The design of 12-bit Pipeline ADC is implemented in LT SPICE schematic editor using CMOS 180nm technology and the results are Simulation with SWTCHER CAD –III. The Overall Design designed is simulating with various input signals and the results are obtained reasonable for the specifications. This 12-bit pipeline ADC is operate up to 15 MHz input frequencies and the Maximum sampling rate get without any missing codes is up to 75 MHz sampling rates. In this paper power dissipation of 3.7mW from Supply Voltage (-1.8V to 1.8V) using analog input (-0.5V to 0.5V) is achieved.

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