Area-Delay and Energy Efficient 2-D DWT Lifting VLSI Architecture for Higher Block Size Image

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ABSTRACT

This paper analyzed the lifting and flipping discrete wavelet transform (DWT) data-path and proposed area delay and energy efficient lifting 2-D DWT VLSI architecture. Theoretical estimate shows that the critical-path-delay (CPD) of lifting cell is higher by 10 AND, OR and Invert (AOI) gates when scaling operations of separated two-dimensional (2-D) DWT are integrated and performed in single step then lifting-based 2-D DWT involves half the number of scaling constants than the flipping-based 2-D DWT. Large number of multipliers are saved into significant saving in multipliers when lifting 2-D DWT is implemented using massively in a parallel structure with integrated scaling. We have derived full-parallel lifting-based 1-level 2-D DWT structure involves M/2 number of less multipliers than the flipping-based 2-D DWT structure. ASIC synthesis result shows that proposed lifting-based structure involve nearly 8% less ADP and 22.5% less EPI than the proposed flipping-based structures on average for block sizes 16 and 32. Compared with the existing lifting-based structure, the proposed lifting-based structures involve 29% less ADP, and 44% less EPI for block size 32, respectively. Compared with existing flipping-based structure, the proposed lifting-based and flipping-based structures, respectively, involve 6.4 times, 5.8 times as little as ADP, and 3.8 times, 2 times as little as EPI for block-sizes 32.The flipping scheme only offers area-delay efficient 2-D DWT structures for smaller block sizes less than 4, where lifting-scheme offers area-delay efficient 2-D DWT structures for block size higher than 4.

Keywords: Critical-path, VLSI Architecture, 2-D DWT, Lifting and Flipping scheme.

I INTRODUCTION

Discrete wavelet transform (DWT) offers a wide variety of useful features such as adaptive time frequency windows, lower aliasing distortion, multi-resolution signal analysis, and efficient computational complexity. Due to these features one dimensional (1-D) DWT and two-dimensional (2-D) DWT are applied in various application such as numerical analysis [1], signal analysis [2], image coding [3, 4)], pattern recognition [5], statistics [6], biomedicine [7] and three-dimensional (3-D) DWT for video processing, volumetric data compression [8]. Multi-dimensional DWT is computationally intensive and many of its applications demand real-time processing for better performance. Therefore, DWT need to be implemented in dedicated very large-scale integration (VLSI) systems for real-time applications. During last two decades, several computation schemes, algorithm mapping, and architectural design methods have been suggested to derive an area-delay efficient VLSI architecture for DWT. These designs are broadly divided into four types as (i) recursive pyramid algorithm (RPA) based design [9], (ii) folded design [10], (iii) parallel design [11] and (iv) pipeline designs [12]. It is observed that the DWT computation scheme affects the performance of DWT structures. Therefore, we discuss here the most commonly used computation schemes in DWT structures.

DWT is a two-channel short-length finite impulse response (FIR) filter-bank, where FIR filters are used in DWT known as wavelet filters satisfy orthogonal property. Few wavelet filters also satisfy bi-orthogonal property [13]. Conventionally, DWT computation is performed using convolution approach. Both orthogonal as well as bi-orthogonal wavelet filter computation are performed using linear convolution. Various VLSI architectures have been suggested for DWT using convolution scheme [14]-[16]. Subsequently, Sweldens [17,18] has proposed a lifting scheme for DWT. The basic principle of lifting scheme is to factorize the poly-phase matrix of a pair of wavelet filters into sequence of alternating upper and lower triangular matrices and a constant diagonal matrix. The lifting based DWT has many useful properties such as symmetric forward and inverse transform, in-place computation, integer-to-integer transform [19]. Most importantly, lifting-based DWT structure involves less arithmetic and memory resources than the convolution based DWT for the same throughput rate implementation .But, lifting scheme is more suitable for bi-orthogonal wavelet filters and involves a longer critical path delay (CPD) than the convolution-based design. Subsequently, Huang et al. (2002) have proposed a modified lifting scheme known as flipping scheme. The flipping scheme is inherently pipelined and it has shorter critical path than the lifting-scheme. Due these feature, flipping scheme is popularly used in most of the recently proposed DWT designs [23] and [26]. It is almost assumed in the literature that, flipping-scheme always gives an area-delay efficient DWT structure. But, we find that the flipping scheme introduces some design complexities in selected DWT structures which make the structure area-delay inefficient compared to the corresponding lifting-based structure. We do not find a detail lifting and flipping data-path study in the literature except the CPD. Therefore, in this paper we

made a detail study on lifting and flipping 2-D DWT data-path to find most appropriate computation scheme to derive area-delay efficient 2-D DWT structure. We also analyzed the critical path of lifting and flipping based DWT structures and made a theoretical estimate of the CPD to quantify the advantage of flipping scheme over the lifting scheme. Based on the data-path study and critical-path estimate of lifting and flipping scheme, we suggest the most appropriate computation scheme to derive area-delay efficient high-throughput 2-D DWT structures. The rest of the paper is organized as: lifting and flipping 2-D DWT data-path study presented in Section 2. Section 3 the proposed full-parallel lifting and flipping structure are presented and in Section 4 presented performance comparison presented and Conclusions are given in Section 5.

II DATA-PATH ANALYSIS OF LIFTING AND FLIPPING 2-D DWT USING INTEGRATED SCALING

(a) lifting scheme for 2-D DWT - Using separable approach 1-D lifting DWT computation is performed row-wise and then column-wise to obtain 2-D DWT output. The multi-level decomposition the low-low sub-band (LL) decomposed into four sub-bands namely low-low (A), low-high (B), high-low (C) and high-high (D) sub-bands. The following set of recursive relations are derived for row-wise computation of the multi-level 2-D lifting DWT for 9/7 filter are as:

$$s_{11}(m,n) = x(m,2n-1) + \alpha(x(m,2n) + x(m,2n-2))$$
$$s_{12}(m,n) = x(m,2n-2) + \beta(s_{11}(m,n) + s_{11}(m,n-1))$$
$$u_h(m,n) = s_{11}(m,n-1) + \gamma(s_{12}(m,n) + s_{12}(m,n-1))$$
$$u_l(m,n) = s_{12}(m,n-1) + \delta\big(u_h(m,n) + u_h(m,n-1)\big) \quad (1)$$

Where α, β, γ and δ are lifting constants. Since the computation of the low-pass and high-pass components of intermediate outputs (u_l(m, n) and u_h(m, n)), respectively, are of similar form, the computation of those components for column-wise computation is expressed as:

$$s_{21}(m,n) = u(2m-1,n) + \alpha(u(2m,n) + u(2m-2,n))$$
$$s_{22}(m,n) = u(2m-2,n) + \beta(s_{21}(m,n) + s_{21}(m-1,n))$$
$$v_h(m,n) = s_{21}(m-1,n) + \gamma(s_{22}(m,n) + s_{22}(m-1,n))$$
$$v_l(m,n) = s_{22}(m-1,n) + \delta(v_h(m,n) + v_h(m-1,n)) \quad (2)$$

Where x(m, n) represents the low-low sub-band components of (j-1)-th level. u(m, n) represents the intermediate output corresponding to the input x (m, n), which could be low-pass and high-pass component u_l(m,n) and u_h(m, n) respectively.

Similarly, v_h (m, n) is the high-pass output corresponding to the intermediate output u_l(m, n) and u_h(m, n) respectively, which respectively, represents a pair of level sub-bands outputs B(m, n) and D'(m, n). v_l(m, n) is the low-pass output corresponding to the intermediate output

$$v_{ll} = A(m,n) = K^2 A'(m,n)$$
$$v_{hh} = D(m,n) = K^{-2} D'(m,n) \quad (3)$$

u_l(m, n) and u_h(m, n) respectively, represent the other two level sub-band outputs A'(m, n) and C(m, n).

The low-pass and high-pass output of lifting 1-D DWT are scaled to normalize their values.

The scale normalization of row and column lifting DWT can be integrated and performed in one step after the column computation, where sub-band outputs B(m, n) and C(m, n) not required scaling while sub-band outputs A'(m, n) and D'(m, n) are scaled by:

(b) Flipping scheme for 2-D DWT - Recursive relations for row-wise computation of the multi level 2-D flipping DWT for 9/7 filter are given as:

$$r_{11}(m,n) = \alpha^{-1}x(m,2n-1) + x(m,2n) + x(m,2n-2)$$
$$r_{12}(m,n) = (\alpha\beta)^{-1}x(m,2n-2) + r_{11}(m,n) + r_{11}(m,n-1)$$
$$u_h(m,n) = (\beta\gamma)^{-1}r_{11}(m,n-1) + r_{12}(m,n) + r_{12}(m,n-1)$$
$$u_l(m,n) = (\gamma\,\delta)^{-1}r_{12}(m,n-1) + \big(u_h(m,n) + u_h(m,n-1)\big) \quad (4)$$

The computation of the low-pass and high-pass components of intermediate outputs (u_l(m, n) and u_h(m, n)), expressed as:

$$r_{21}(m,n) = \alpha^{-1}u(2m-1,n) + u(2m,n) + x(2m-2,n)$$
$$r_{22}(m,n) = (\alpha\beta)^{-1}u(2m-2,n) + r_{21}(m,n) + r_{21}(m-1,n)$$
$$v_h(m,n) = (\beta\gamma)^{-1}r_{21}(m-1,n) + r_{22}(m,n) + r_{22}(m-1,n)$$
$$v_l(m,n) = (\gamma\,\delta)^{-1}r_{22}(m-1,n) + \big(v_h(m,n) + v_h(m-1,n)\big) \quad (5)$$

The scale normalization of row and column flipping DWT can be performed after the column computation, where sub-band outputs A'(m, n), B′(m, n), C′(m, n) and D'(m, n) are scaled by:

$v_{ll} = A(m,n) = (\alpha\beta\gamma\delta K)^2 A'(m,n)$

$v_{lh} = B(m,n) = (\alpha\beta\gamma)^2 \delta B'(m,n)$

$v_{hl} = C(m,n) = (\alpha\beta\gamma)^2 \delta C'(m,n)$

$v_{hh} = D(m,n) = (\alpha\beta\gamma/K)^2 D'(m,n)$ (6)

III PROPOSED FULL-PARALLEL LIFTING AND FLIPPING 2-D DWT STRUCTURES

(a) Proposed Structure - The proposed structure for lifting and flipping 2-D DWT is shown in Fig. 1. It consists of one row processor and one column processor. The column processor is composed of one low-pass block and one high-pass block. During every cycle, the row-processor receives 2M samples corresponding to two successive columns of input matrix such that the entire input matrix of size (M × N) is fed to the row processor in N/2 cycles. The row processor produces one column of low-pass one column of high-pass intermediate matrices of sizes (M × N/2) in every cycle. The structure of row-processor for lifting 2-D DWT is shown in Fig. 2 and for flipping 2-D DWT is shown in Fig.3. Both these structures have different scaling unit for lifting and flipping cell.

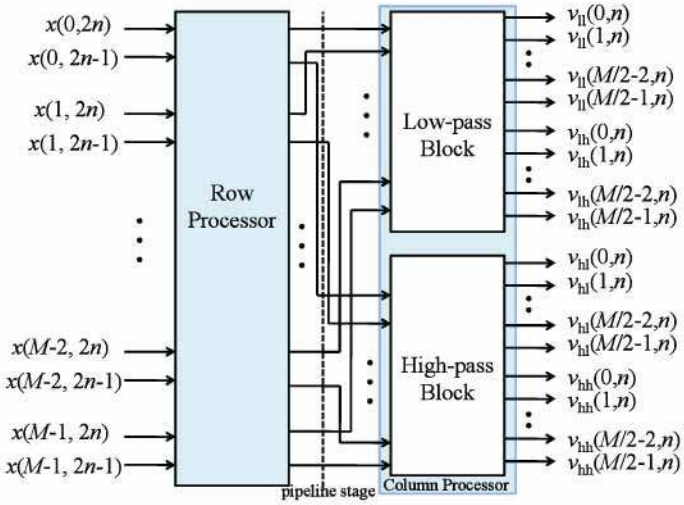

Fig.1 Proposed full parallel structure for lifting and flipping 1-level 2-D DWT

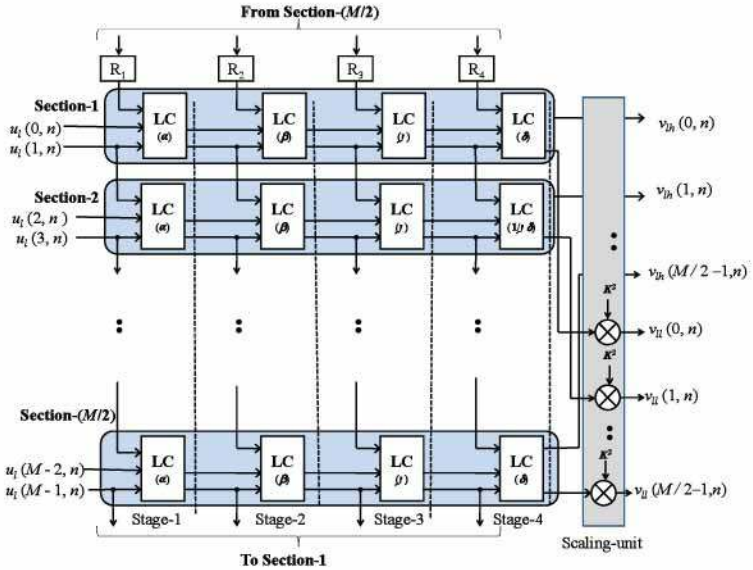

Fig.2 Structure of row processor unit of lifting 2-D DWT

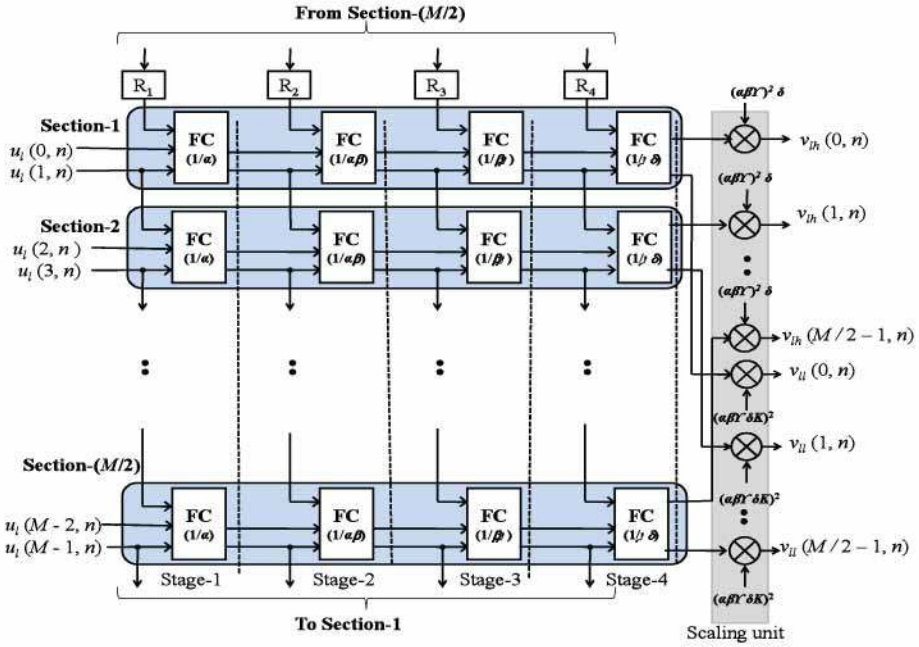

Fig. 3 Structure of row processor unit of flipping 2-D DWT

Now column processor receives data directly from the row-processor without any data transposition. During every cycle, the column processor receives one column of low-pass intermediate matrix and one column of high-pass intermediate matrix in parallel such that the low-pass block of column-processor receive columns of low-pass intermediate matrix and the high-pass block receive columns of high-pass intermediate matrix. The low-pass block produces one column of each pair of sub-band matrices low-low and low-high, where the high-pass block produces one column of other two sub-bands high-low and high-high. The structure of low-pass block of lifting and flipping 2-D DWT are shown in Fig.4(a) and Fig. 4(b), where the structure of high-pass block of lifting and flipping 2-D DWT are shown in Fig.5(a) and Fig. 5(b).

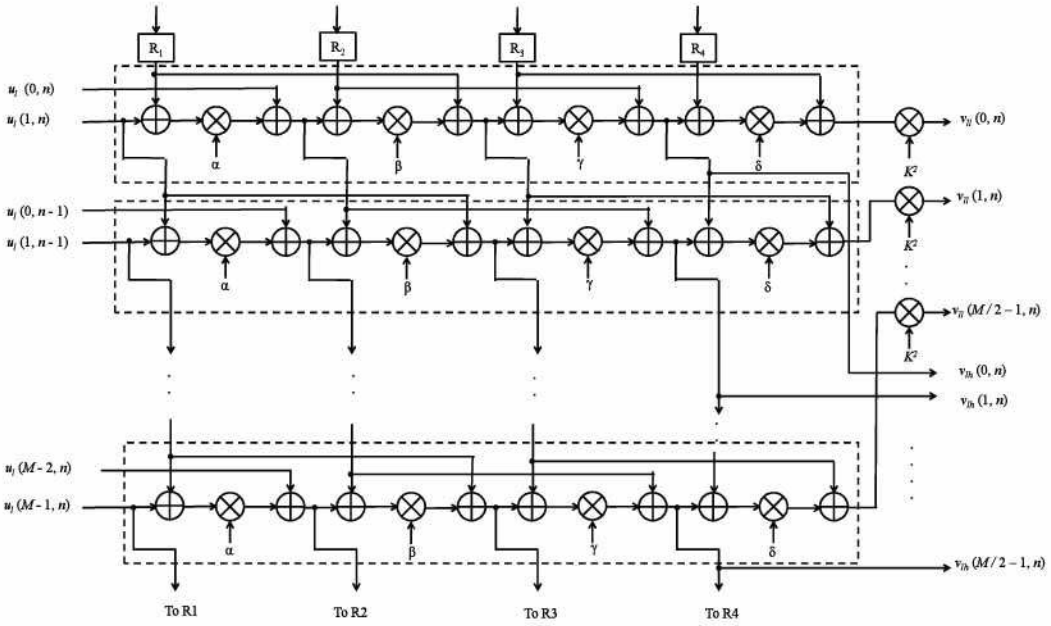

Fig.4(a) Structure of Colum Processing low-pass unit of lifting 2-D DWT

As shown in Fig.4 and Fig.5, both the low-pass and high-pass blocks of lifting and flipping 2-D DWT are identical except the scaling constants. Both the low-pass and high-pass block of lifting 2-D DWT involves M/2 multipliers each for scaling the sub-band components while the low-pass and high-pass block of flipping 2-D DWT involves M multipliers each for the same operation. Therefore, the full-parallel lifting 2-D DWT structure involves M less multiplier than the flipping 2-D DWT structure. Parallel structure for block size P < 2M (full-parallel structure) also can be derived similar to the proposed full-parallel structure for both lifting and flipping 2-D DWT. In those cases, lifting 2-D DWT structure involves P/2 less multipliers than the flipping 2-D DWT structure. Since, critical-path of lifting cell is marginally higher than flipping cell, area-delay efficiency of lifting 2-D DWT structure would be better than flipping structure for higher block sizes.

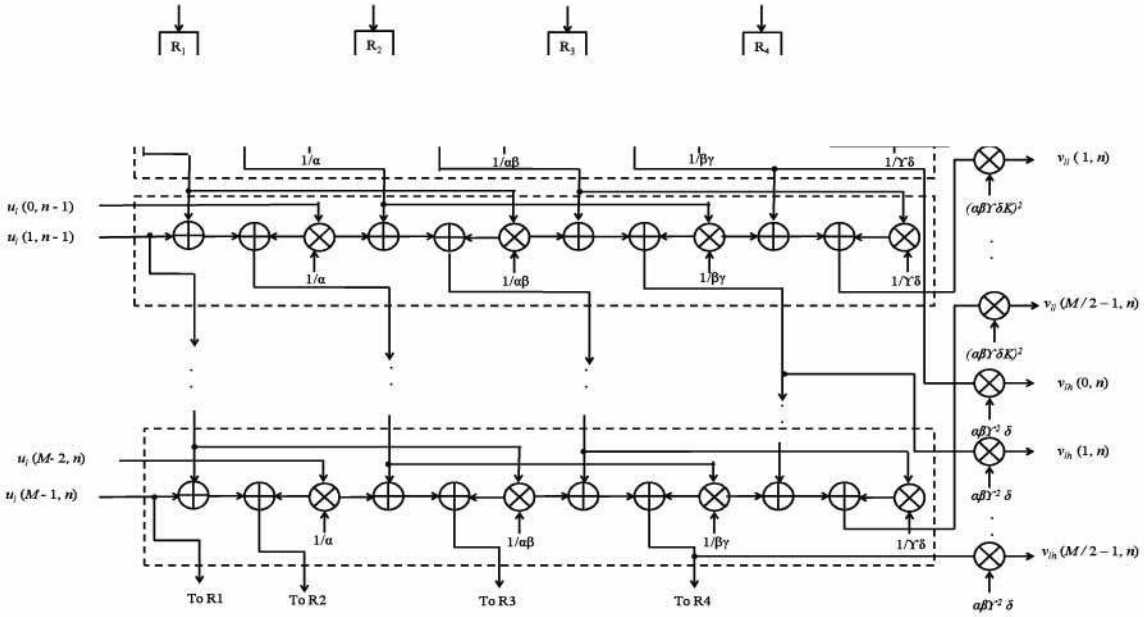

Fig.4(b) Structure of Colum Processing low-pass unit of Flipping 2-D DWT

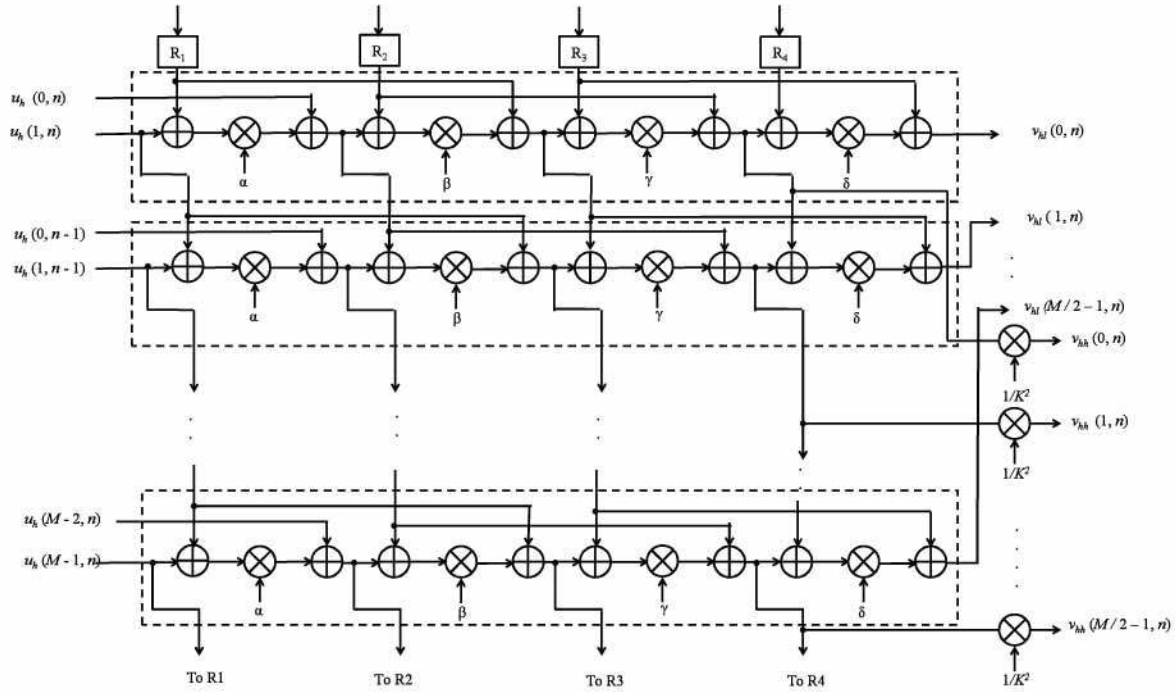

Fig. 5(a) Structure of Column Processing high-pass unit of Lifting 2-D DWT

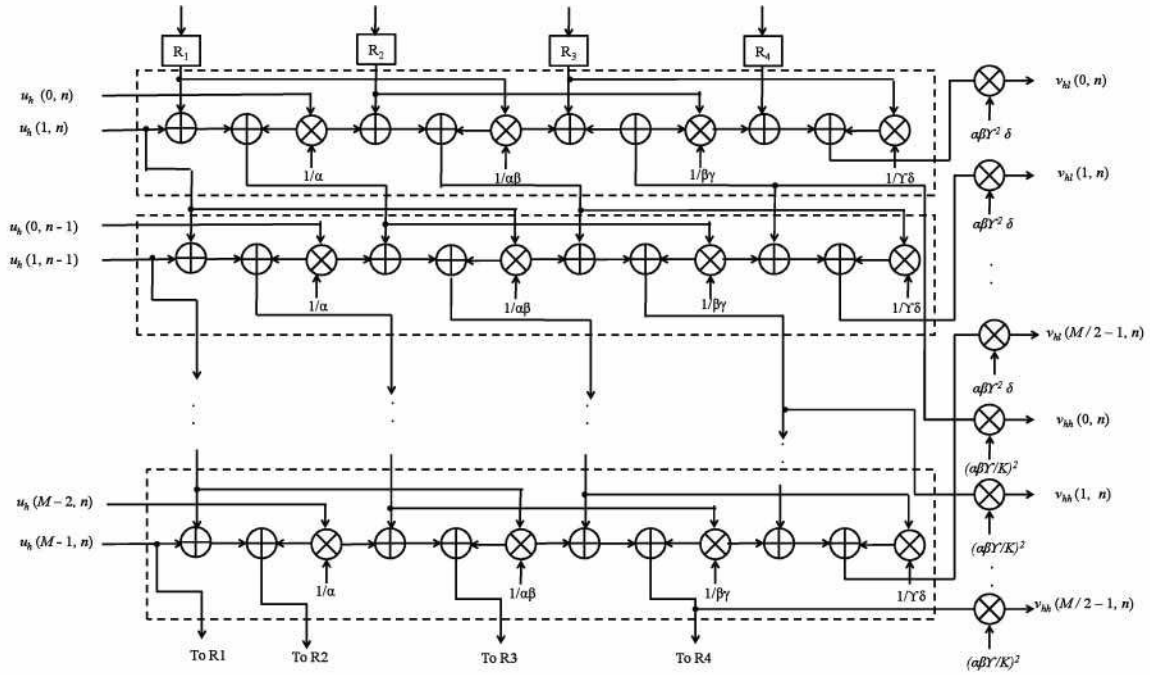

Fig. 5(b) Structure of Column Processing high-pass unit of Flipping 2-D DWT

From the above Fig. 4 (a) and (b), low-pass unit of column processor for lifting scheme require M/4 less multiplier than the flipping scheme of the scaling unit. Similarly high pass unit of lifting scheme require M/4 less multiplier over flipping scheme also (shown in Fig. 5 (a) and (b)). Therefore we have seen that the total number of multiplier saving in lifting scheme M/2 over flipping scheme.

(b) Hardware - time complexity and performance considerations - We have considered the existing lifting structures [23] and flipping structure of [18] for comparison as these structures have the same frame buffer complexity for the same throughput (number of DWT components per cycle). Note that the proposed lifting-based and the structure proposed in [23] are identical for the same throughput implementation. Therefore, these two structures are assumed to be one structure for comparison purpose.

We have estimated hardware complexity of the proposed structures for different throughput. The theoretically estimated values of proposed structures and existing structures of [23] and [18] are listed in Table 3 for comparison purpose in terms of multiplier, adder and on-chip memory words for hardware complexity and cycle period (in terms of AOI gate counts) and throughput rate for time complexity.

As shown in Table 3, the proposed lifting based structures and the existing structure of [23] have the same multiplier, adder and time complexity for the same throughput rate, except that the proposed lifting based structure involves 1.5N less on-chip memory words than those of [23]. Compared with the structure of [23], the proposed flipping based structure for the same involve the same number of adders and on-chip memory words, but it involves 8 and 16 number of more multipliers than those of [23] for throughput rate 16 and 32 samples per cycle, and its cycle period is less by 10 AOI gate delays. Compared with the structure of [18], the proposed lifting-based structure involve 7.2 times and 14.4 times more multipliers, 8 times and 16 times more adders and offers 8 and 16 times higher throughput, respectively. However, the proposed lifting structure has marginally longer cycle period by 10 AOI gate delays than that of [18]. When the proposed lifting structure is compared with the proposed flipping structure, then we find that the proposed lifting structure, for throughput rate 16 and 32 involve 8 and 16 less number of multipliers, respectively, but it has a longer cycle period than the flipping structure by 10 AOI gate counts. Since, both the proposed lifting and flipping structures have the same on-chip complexity and it is independent of throughput rate, the area saving offered by the proposed lifting structure over the proposed flipping structure is substantially higher than the delay penalty due to longer critical path of flipping structure. Therefore, the area-delay efficiency of the proposed lifting structure is expected to be better than the proposed flipping based structure as well as the existing similar structures.

Table 3

Comparison of Hardware and time complexity of proposed structure and existing lifting and flipping based 2-D DWT structures

Structures	Scheme	Throughput per cycle	Multiplier	Adder	Cycle period (AOI gate counts)	On -chip memory (words)
Structure of [18]	Flipping	2	10	16	64	$4N + 44$
Structure of [23]	Lifting	16	72	128	77	$5.5N$
	Lifting	32	144	256	77	$5.5N$
Proposed	Lifting	16	72	128	77	$4N$
	Lifting	32	144	256	77	$4N$
Proposed	Flipping	16	80	128	67	$4N$
	Flipping	32	160	256	67	$4N$

IV PERFORMANCE COMPARISION

We have coded proposed structures and the structure of [23] in VHDL for block sizes 16 and 32. We also coded the structure of [18] in VHDL. We have assumed 1-level decomposition of the input image of size (512×512) and synthesized all the designs without frame-buffer as the frame-buffer usually external to the chip due to its large size compared to the core. We have considered 8-bit pixel and 12-bit word length for intermediate and output signals. All the designs are synthesized in Synopsys Design Compiler using SAED90nm CMOS library [25]. Area, minimum clock period (MCP) and power reported by the Design Compiler are listed in Table 4 for comparison. Power is estimated at the MCP of respective designs.

Table 4

Synthesis results of lifting and flipping based existing and proposed 2-D DWT structures

Structures	Scheme	Throughput Per cycle	Core Area (μm^2)	MCP (ns)	ADP (μm^2.ns)	Core Power (mw)	EPI (μJ)
Structure of [18]	Flipping	2	699798.06	17.67	1620.76	15.13	35.04
Structure of [23]	Lifting	16	1295885.83	22.00	467.09	91.38	32.93
		32	1713209.02	23.10	324.19	118.78	22.47
Proposed	Lifting	16	1046304.33	20.64	353.82	66.62	22.52
		32	1500121.84	20.74	254.87	73.52	12.49
Proposed	Flipping	16	1198201.36	19.75	387.71	98.97	32.02
		32	1699056.77	19.94	277.53	106.32	17.36

Legend : ADP: Area-delay-product, ADP = Core Area × MCP × CT, EPI: Energy per image, EPI = Core power × MCP × CT, CT: computation time = Image size/ Block size

As shown in Table 4, the structure of [18] has lowest MCP than other designs due to smaller critical path as given in the theoretical estimate of Table 3. The proposed lifting-based structure involves 12.67% and 11.7% less area than the proposed flipping-based structure for block size 16 and 32, respectively. This is mainly due to saving in multipliers in the lifting structure. Compared with the lifting structure of [23], the proposed lifting based structures involve 23.8% and 14.2% less area and flipping-based structure involve 8% and marginally less area for block size 16 and 32, respectively. Compared with the flipping structure of [18], the proposed lifting-based structure involves 1.5 and 2.2 times more area and offers 6.84 times and 13.6 times higher throughput, respectively. The proposed flipping-based structure involves 1.7 times and 2.4 times higher area than the structure of [18] and offers 7.15 times and 14.15 times higher throughput than other.

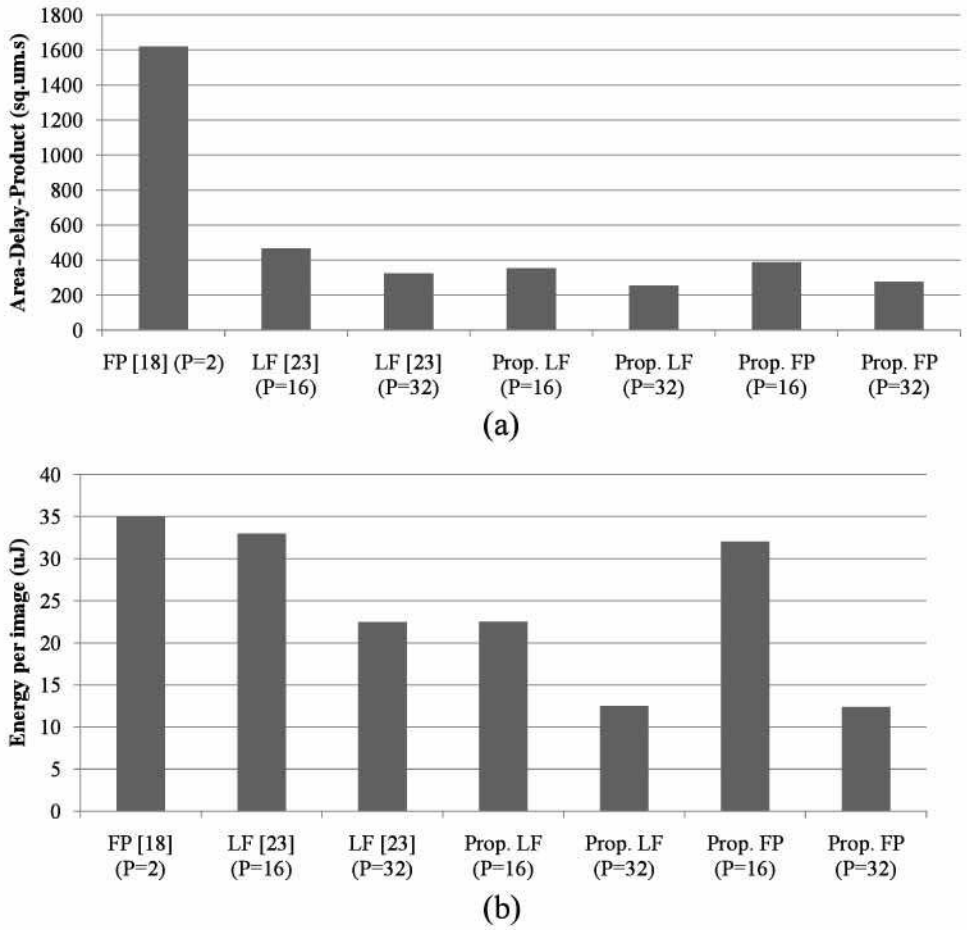

Fig. 6(a) Comparison of area-delay-product. (b) Comparison of energy per image (EPI). LF stands for lifting and FP stands for flipping.

We have estimated area-delay product (ADP) (ADP= Area × MCP × Image-size / block-size) and energy per image (EPI) (EPI = Power × MCP × Image-size / block-size) of all the designs listed in Table 4. The estimated ADP and EPI values are shown in Fig. 6 (a) and Fig. 6 (b) in terms of bar-chart. As shown in Fig. 6 (a) and Fig. 6 (b), the proposed lifting-based structure involves nearly 8% less ADP and 22.5% less EPI than the proposed flipping-based structure on average for blocks sizes 16 and 32. Compared with the structure of [23], the proposed lifting-based involve 24%, 29% less ADP, and 39%, 44% less EPI for block sizes 16 and 32, respectively. Similarly, the proposed flipping-based structure involve 16%, 14% less ADP and 3%, 22% less EPI than those of [23] for block sizes 16 and 32, respectively. Compared with the structure of [18], the

proposed lifting-based structure involve 6.4 times less ADP and 3.8 times less EPI for block-sizes 32. For the same block-size, the proposed flipping-based structure involve 5.8 times less ADP and 2 time less EPI than those of [18].

V CONCLUSION

In this paper, we made an analysis on the data-path of lifting and flipping 2 –D DWT. The analysis reveals a novel concept, that scaling constants of lifting DWT are perfectly inverse of each other while those of flipping DWT are not. Theoretical estimate shows that the CPD of lifting cell is higher by 10 AOI gates. Since, scaling constants of lifting DWT are perfectly inverse of each other, scaling operations of row and column DWT when integrated in 2-D processing, then lifting-based 2-D DWT involves half the number of scaling constants than those flipping-based 2-D DWT. This results into significant saving in multipliers when lifting 2-D DWT implemented in a parallel structure. We have derived full-parallel lifting-based and flipping-based 2-D DWT structures and shown that the lifting-based 1-level 2-D DWT full-parallel structure involves M/2 number of less multiplier than the similar flipping-based 2-D DWT structure. ASIC synthesis results the proposed lifting-based structure involve nearly 8% less ADP and 22.5% less EPI than the proposed flipping-based structure on average for block sizes 16 and 32. Compared with the structure of [23], the proposed lifting-based structure involves 29% less ADP, and 44% less EPI for block size 32, respectively. Compared with flipping-based structure of [18], the proposed lifting-based and flipping-based structures, respectively, involve 6.4 times, 5.8 times less ADP, and 3.8 times, 2 times less EPI for block-sizes 32. Therefore, flipping-scheme no longer gives an area-delay and energy efficient structure when 2-D DWT implemented in parallel structures for higher block-sizes image.

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