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Review on Custom and Semicustom Designs for Multibit Arithmetic Logic Units Using CMOS

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ABSTRACT
In this paper authors have presented an extensive review on literature on designing of multibit arithmetic logic units based on custom and semicustom techniques. A brief review is carried out for proposed design and will be done using MOSIS C5 process for VLSI. Arithmetic Logic Unit is a digital circuit that performs arithmetic and logical operations. ALU is a fundamental building block of central processing unit of a computer which is used in the simplest microprocessors for purpose of maintaining timers. Previously, many efficient architecture have been introduced for the design of low complexity operation, but we have given attention to custom designing of ALU , where every sub module is designed simulated and verified then routed accordingly. The proposed design of ALU will performs the mathematical, logical, and shifting operations like Addition, Subtraction, Multiplication, Increment, Decrement, Logical AND, Logical OR, Logical XOR etc. in the computer. In this paper, the efficient modules of ALU will be design using Custom Tools like Electric CAD and simulation results will be verified on same platform using test benches and SPICE simulations.

Index Terms—ALU, CAD for VLSI, Process technology, Custom and Non custom VLSI techniques.

I INTRODUCTION

An ALU that can perform: A AND B, A OR B, A + B (addition), and A - B (subtraction) and all possible arithmetic and Logical operations. In most designs as our reference design a bit arithmetic logic unit as shown in the below figure supports addition, 2's complement subtraction, overflow detection, bitwise invert, bitwise logic AND, bitwise logic OR and bitwise logic XOR operations. The high level circuit diagram of the four-bit ALU is as as shown in figure 1.

As we can see from Figure 1, the diagram can be roughly divided into four sections. They are arithmetic section (blue), overflow section (yellow), logical section (red) and selection section (green). The blue section is a chain of full adders. It is responsible for addition (ADD), subtraction (SUB) and invert (INV) operations. The ADD operation requires Binv set to low, such that it functions like a ripple adder. For SUB operation, it uses 2's compliment and thus, A-B becomes A + (-B). The usage of Binv has two folds

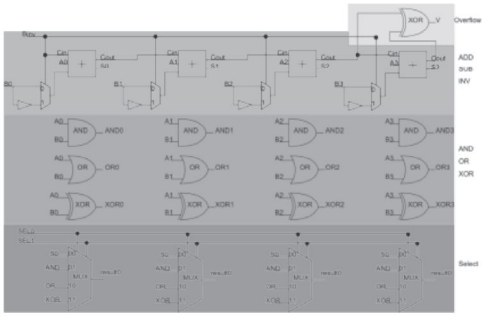

Fig. 1: High level circuit diagram of the four-bit ALU

Firstly, when Binv is high, B will be inverted (through the inverter and MUX) before going into the full adder. Secondly, Binv also serves as the initial carry-in for 2's complement. To perform bitwise INV, input A needs to be set to zero and Binv set to high to invert input B. As a result, B first got invert to -B and the operation becomes 0 + (-B) = -B. The yellow section reports if there's any overflow occurs throughout an operation. Overflow happens when adding two positive numbers but the result is negative (the most significant bit is 1). For instance, 0101 + 0011 = 1000, the resulting value 1000 is negative in 2's compliment, so overflow has occurred. We want to set the overflow bit (V) to high when such situation happens. The carry out from last two full adders can be XOR together. The result would be the overflow bit. The red section performs bitwise logical operations, including AND, OR and XOR. Since each gate handles only one bit, in order to handle four-bit inputs, we need to place four gates of the same kind in parallel. The green section is select section, which determines which operation results go to the output. There are two bit select line (SEL0, SEL1) that select different operations.

The ALU proposed will implement the AND, OR, Addition, and Subtraction functions for the 8-bit A and B input buses and the result will be output to the 8-bit bus.

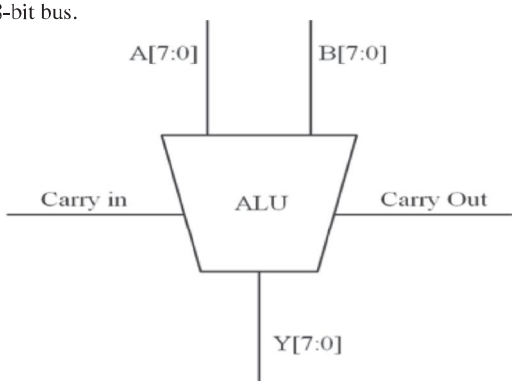

Fig. 2 General block diagram of 8 Bit ALU

II RELATED WORK

The designing of high performance analog and digital integrated circuits is becoming most essential with the continuous trend toward the reduced supply voltage and transistor channel length. MOS is the most success among all because it can be scaled down to smaller dimensions for higher performance. The size can be reduced to micrometer or nanometer for getting higher performance

In [1] Kumbhalkar, Snehal, and Sanjay Tembhurne in their paper entitled, " a novel arithmetic logic unit design for delay & area optimization" proposed the design and implementation of an Arithmetic Logic Unit (ALU) using area optimizing techniques such as Gate Diffusion Input (GDI) and transmission Gate (TG). On the bases of review project they are designing 4bit-ALU by mix designing technique to reduce delay then conventional CMOS 4bit-ALU by using TANNER15.0 EDA tool. This 4bit-ALU will design in 0.18µm technology with 1.8V supply voltage.

They concluded that to reduce power consumption GDI is efficient technique it reduces the number of power supply to ground connections which reduces minimum power consumption and minimum area to implement design. This GDI technique used to design Full adder circuits

The advantage of transmissions gate in some circuit can be explained by the fact that one nMOS and one pMOS transistor is conducting at once for each logic state in transmission gates. So TG can be used for designing the multiplexer circuit in the ALU.

In [2] Vivechana Dubey and Raviohan Sairam "An Arithmetic and Logic Unit optimized for Area and Power" 2014IEEE Forth International Conference On Advance Computing & communication technology. This paper based on 0.25µm CMOS technology is used with 1.8V power supply and simulation is done using TANNER EDA 13.0 simulator using TSMC BSIM. In this 4-bit ALU is design to meet the low power and minimum area. In today's CMOS circuit's dynamic power dissipation is the main factor which causes power dissipation in CMOS circuits. So in this paper number of power supply to ground are reduced in GDI implementation which reduces the dynamic power consumption. Whole representation of ALU is design by GDI technique& various topologies of multiplexers and full adder implementation is studied and compared. The 2x1 mux, 4x1 mux, 1-bit full adder with 10-transistor designed using GDI technique is chosen for lowering power consumption and minimum area. After simulation number of transistor for 4bit ALU with CMOS gate- 592, ALU with transmission gate and 10 transistor full adder- 416 & Proposed 4bit-ALU with GDI based full adder- 232.

Power Consumption:- 4bit-ALU, Number of CMOS gate- 4204.5µW, ALU with transmission gate and 10 transistor full adder- 1197.5µW. Proposed 4bit-ALU with GDI based full adder-1030.5µW.

In [3] Arvind Kumar "Comparative Study of 4-Bit ALU using CMOS and BiCMOS for 200nm Technology" In this paper, the design of a high performance 4-bit ALU using CMOS & BiCMOS technologies for high speed applications. These were further compared w.r.t. speed, power dissipation and power delay product. The comparison of CMOS to BiCMOS often seen in the literature shows the delay of single stage circuits driving a capacitive load, with the BiCMOS circuit exhibiting a bold advantage. TANNER EDA tools were used for schematic simulation.

The simulation technology used was MOSIS 200nm. This ALU can be used in mixed signal processing like radar system, image recognition, high speed broadband networks etc. The analog input signal must first be sampled and digitized using an ADC (analog to digital converter). The resulting binary numbers, representing successive sampled values of the input signal, were transferred to the processor. The ALU of the processor carried out numerical calculations with them. These
Calculations typically involve multiplying the input values by constants and adding the products together.

Comparative Study on each operation is performed for 4 bit ALU. Delay, number of transistor and power delay product are also compared to CMOS and BiCMOS.

In [4] paper, the multiplication unit of alu is designed using a process of calculation based on set of 16 sutras i.e. (Vedic Mathematics). Based on this technique the structure of 2bit, 4bit and 8 bit multipliers based on vedic approach redisplayed and is encoded in a VHSIC Hardware Description language (VHDL) and synthesized with the aid of EDA tool, XilinxISE12.2i. Finally, an evaluation of differences is made across the results placed by Vedic design with traditional multipliers.

In [5] the prototype and purpose of the various tasks carried out by a reconfigurable ALU are described. On precision presentation representing the location of decimal point by exponent of radix, addition and subtraction of 32 bit is taken. It can be helpful in parallel processing approach and computation intensive applications. The design is for 32 bit input system can be utilised in multimedia applications. As frequency decreases, the power consumption also decreases without taking IO standard into consideration.

In [6] the synchronous crucial algorithm is utilised, where both the transmitter and receiptant utilise a sole principle of encoding as well as decoding is AES. The declared structure is improved as compared to the Look-up table way, as arena filled by Lookup table technique is much farther along the extent of a Xilinx Spartan 3E series of FPGA. In status of timing approach, a contrast in time with LUT way is surplus, taking its major space habitation. When taking the status of logic gates, this technique occupies 46 XOR gates only.

In [7] Area Gated Diffusion Input Technique is a latest option for reduction in power dissipation and propagation hold up. There are three inputs in a GDI cell - G (NMOS and PMOS common gate input), P (PMOS, input to the source/drain) and N (NMOS, input to the source/drain).A major part of both NMOS and PMOS are joined to N and P respectively. The design utilise the idea of GDI (Gated diffusion input) approach in the implementation of ALU and its sub areas as Multiplexers and Full adders. Less dynamic power usage as power supply to ground connections is minimum in GDI design technique.

In [8] the Floating point integers are commonly written as ((1)S)(F)(2E),where F shows a digit in fraction value, where E shows a digit in the exponent value. In widespread, mantissa value is assigned by addition of 1 as MSB. In case where the exponent value is big enough that it cannot be handled by exponent field then an overflow flag becomes high. In the situation where the negative exponent is big enough to fit the exponent field, then an overflow flag is shown. IEEE-754 standard started a new method known as NaN (Not a Number), for the functions that are not valid and are condition when zero is divided with zero, subtraction of infinite number from infinite one. Karatsuba algorithm used progressively for the need in such applications is explained. An impressive multiplication algorithm, which helps in accurate usage of input output pins and with reduced delay should be utilized for proper design of floating point processors. In binary system, floating point integers are defined in two ways namely, single and double precision. These formats are characterized by exponent, mantissa and sign fields. On the basis of device usage and output valuation, Vedic multiplier advanced over Karatsuba multiplier both for single and double precision formats. Even though Booth multiplier adapt minimum resources, it is also low in speed.

In [9] there is a new approach used for energy optimization that is low voltage complementary metal oxide semiconductor technique.LVCMOS12, LVCMOS15, LVCMOS18 and LVCMOS25 are various options of LVCMOS relying on their supply voltage of output driver. The output evaluation shows a energy optimization as using LVCMOS12 and LVCMOS15 instead of LVCMOS 25 is 68.34% and 52.51%. All the values are calculated in Verilog language with behavioral simulation and ISim in Xilinx 13.4 ISE and all code can be synthesized on virtex-6 FPGA. Further it also states that in term of power expenditure LVCMOS is one of the best IO standard and Virtex-6 is the well power planned FPGA.

In [10] The Co-existence of CMOS and SET (Single Electron Transistor) is the latest trend in the era of advanced semiconductor industry. In the paper we are given with the robust execution of ALU (Arithmetic Logic Unit) with the help of hybrid SETCMOS, also utilising hybrid SET-CMOS based logic gates that are reversible in nature. The simulation of results of given both cases are made with an estimate of similarities and dissimilarities made between them by using various approaches. In this paper ALU design of 4 bit hybrid SET-CMOS based ALU and 4 bit hybrid SET-CMOS Reversible logic gate. It can be concluded that hybrid SET-CMOS based Reversible logic is better in operation in contrast to conventional CMOS design and realizes the target of low power expenditure.

In [11] the paper presents a well planned and operational designing the asynchronous ALU with reduction of delay for the execution of instructions on FPGA. With the help of 4 way handshaking protocol we can decrease the delay and get large pliability and execution of the arithmetical and logical unit. The design methodology utilized is asynchronous. The work proposes the ALU, attempts to reduce the fundamental drawbacks of the synchronous design of ALU, viz. clock skew, power expenditure and detention by utilising the asynchronous ALU but the major limitations is large LUT consumption.

In [12] when computation for large number of bits in ALU is required, there is a need of cascading the adder circuit. These Cascaded adders however lead to Carry Propagation Delay (CPD) thereby affecting the speed of operation. 8 Bit, 16 Bit, 32 Bit and 64 Bit ALU is proposed using modified SQRT CSLA and also implemented ALU using modified SQRT CSLA by CLA. For realizing higher bit ALU using regular/modified SQRT CSLA, cascade methodology can be used. The ALU design and implementation using modified SQRT CSLA shown for low power and area-efficient applications. By introducing CLA in ALU better performance is obtained in terms of speed.

In [13] the one to one correspondence is the actual key required for reversible circuits that should count input and output pins equal. In other words every state of input should be consumed for particular output that is output logic will be shared by only one input logics present. A number of AND gates as well as adder units have been used to design a conventional multiplier, which also produces a remarkable delay. A time worthy approach for the resultant by using reduced count of resources is by using vedic algorithm, thereby effective delay decrement while gradual enhancing the rate of execution of output. The proposed implementation overcome power as well as delay hardcore bring forth by Selective Reversal as well as rapid algorithm of Vedic Method.

In [14] to design the two bit multiplication unit i.e. multipliers are proposed to obtain the result of two n-bit binary integers and then execute it on a Nexys 3, Spartan 6 FPGA kit is the principal purpose. Binary multiplication units of 32x32 have been evaluated with traditional multipliers depending on their result obtained at the execution after the final design. A list of evaluation is made based on 32-Bit Vedic mathematics based multiplier unit and a Conventional Binary Multiplier. It has been seen that the number1I0s required for 32-bit Vedic mathematic based multiplier unit and other binary multipliers are 128 out of 232, therefore out of which the requirement becomes 55% for both of the multipliers.

Table 1
Comparison Table for Review

Author	Paper Topic	Remark
Kumbhalkar, Snehal, and Sanjay Tembhurne	a novel arithmetic logic unit design for delay & area optimization	GDI technique for power reduction 0.18µm Tool TANNER15.0 EDA
Vivechana Dubey and RaviohanSairam	Arithmetic and Logic Unit optimized for Area and Power	ALU is design by GDI technique& various topologies of multiplexers, 0.25µm Tool : TANNER EDA 13.0 simulator using TSMC BSIM
Arvind Kumar	**4-Bit ALU using CMOS and BiCMOS**	**4 bit ALU. Delay, number of transistor and power delay product are also compared to CMOS and BiCMOS, MOSIS 200nm Tool : Tanner EDA**
Garima Rawat, Khyati Rathore, Siddharth Goyal, Shefali Kala	Multiplication unit of ALU	Vedic design with traditional multipliers. Tool Xilinx ISE
Begum, J. Thameema, S. Harshavardhan Naidu, N. Vaishnavi, G. Sakana, and N. Prabhakaran	Design and Implementation of Reconfigurable ALU for Signal Processing Applications.	Design is for 32 bit input sytem Tool Xilinx ISE
M Senthil kumar,Dr S Rajjalakshmi	''High Efficient Modified MixColumns in Advanced Encryption Standard using Vedic multiplier.	Structure is improved as compared to the Look-up table way , as arena filled by Lookup table technique Tool Xilinx ISE
Pandey, Bishwajeet, Jyotsana Yadav, Yatendra Kumar Singh, Ravindra Kumar, and Surabhi Patel	Energy efficient design and implementation of ALU on 40nm FPGA	in term of power expenditure LVCMOS is one of the best IO standard and Virtex-6 is the well power planned FPGA Tool Xilinx ISE
Jana, Biswabandhu, Anindya Jana, Subhramita Basak, Jamuna Kanta Sing, and Subir Kumar Sarkar.	Design and performance analysis of reversible logic based ALU using hybrid single electron transistor.	Robust execution of ALU with the help of hybrid SETCMOS. hybrid SET-CMOS based Reversible logic is better in operation in contrast to conventional CMOS design and realizes the target of low power expenditure.
Bhandari, Nikhil, and Shubhajit Roy Chowdhury	FPGA based High Performance Asynchronous ALU based on Modified 4 Phase Handshaking Protocol with Tapered Buffers	The work illustrates the ALU, that attempts to reduce the fundamental drawbacks of the synchronous design of ALU, viz. clock skew, power expenditure and detention by utilising the asynchronous ALU but the major limitations is large LUT consumption.
Nautiyal, Priyanka, Pitchaiah Madduri, and Sonam Negi	"Implementation of an ALU using modified carry select adder for low power and area-efficient applications	The ALU design and implementation using modified SQRT CSLA shown for low power and area-efficient applications. By introducing CLA in ALU better performance is obtained in terms of speed.
Kunal adav, Aditya vibute and Shyam Iyer Novel	Vedic Mathematics Based ALU using application specific reversibility	The proposed implementation overcome power as well as delay hardcore bring forth by Selective Reversal as well as rapid algorithm of Vedic Method

Arvind Kumar in his paper [3] presented a study of 4 bit ALU using CMOS and BiCMOS 200 nm process technology. They presented a custom approach to design ALU which will also be our proposed methodology. The simulation technology used was MOSIS 200nm.The proposed work will include

50nm and 300nm MOSIS models for the design of ALU. This ALU can be used in mixed signal processing system

III PROPOSED METHODOLOGY

Defining the requirements and setting the specifications is an important aspect if any VLSI Design. Design of the proposed 8 bit ALU will be according to the Tool flow (EDA based). The proposed methodology will start with the design of the test circuits like basic gates, for example NOT Gate, NAND gate, NOR gate etc followed by simulating the test results and optimization of transient and DC characteristics for the sub circuits. A pad frame is also proposed that will accommodate all ALU sub circuits and will be approximately 40 – 60 pins. The process

technology used here is c5 process provided by MOSIS.

The technology used in Electric is C5 process, 300 nm and is also used for fabrication is with respect to MOSIS design rules. This process has two layers of polysilicon to make a poly1 -poly2 capacitor, 3 layers of metal, and a hi-res layer to Design of Digital ALU. The system in whole is designed in various steps. Firstly, the basic sub modules of the system are designed. The design procedure of these sub modules involves obtaining the Boolean expression for the operation to be performed. When the Boolean expression is obtained, the CMOS schematic is prepared for the same. The sources and drains are marked for the PMOS and NMOS. The step following the schematic design is the layout design. Layout design is very important part of the pad frame digital design. The design uses Euler's Rule for finding the best arrangement of input gates and obtaining minimum number of interconnects. The design of CMOS combinational circuits starts with the very basic design of NMOS and PMOS. The active regions for the MOS, the MOS itself and the wells are positioned based on the design rules and requirements. The design rule checks need to be applied after every step so that errors, if occur, can be removed. As we make progress in design technology, there is a ongoing debate within the design technology community about the importance of new algorithms and tools or new methodologies and associated tool flows. The simple fact is that history of design for microelectronic systems includes the going of both of them hand in hand to get the maximum benefit and in act these two aspects of the design technology are tightly coupled and correlated in terms of their impact.

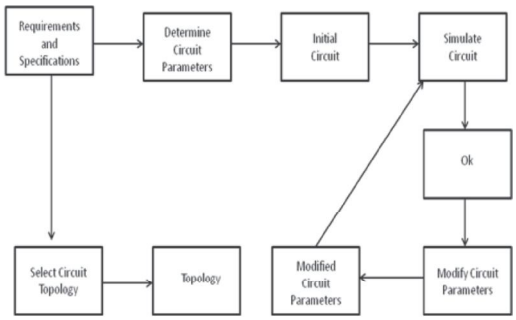

Fig. 3 VLSI CAD/EDA design methodology

VLSI Design incorporates both the design methodologies and associated CAD tools because both forms the integral parts and should go hand in hand as they evolve based on the designer's needs.

IV WORK TILL NOW

Designing an ALU and peripheral circuits with the high reliability and yield as well as this must meet the design and performance requirements. Design of a 8 bit digital ALU will use 300 nm and 50nm process technologies, 2 metal layer process for design. Physical design of digital gates and a 40 pin pad frame is also proposed alongside the overall analysis. A part of the proposed work and pad frame is as shown

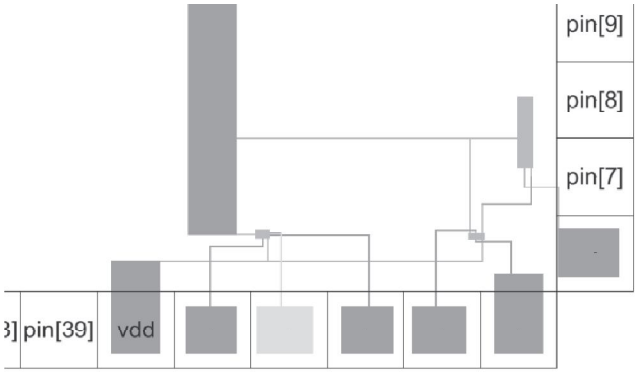

Fig. 4 Design padframe till now

V CONCLUSION

Arithmetic Logic Unit is a critical component of a microprocessor or digital entity. An efficient module for design of the ALU has been discussed through various literatures. After thoroughly studying these literatures it has been concluded that the techniques which acquired are quite effective to improve the parameters of designed module of multi-bit ALU. These help in optimizing the system by using efficient techniques. The ALU design using carry look ahead and reversible logic gate approach increase the speed to a great extent but it results in increased hardware complexity. The proposed methodology will provide a systematic way to derive high speed system at a very less area. We have proposed the physical design model of multibit ALU with efficient design approach using less area, high speed methodology. Also, Author efforts will be directed towards implementation of n bit ALU design with different circuit topology.

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