Analysis of Leakage Power Suppression Technique for CMOS VCO in 45nm Technology

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ABSTRACT
This paper proposed SVL self voltage level technique for the designing of VCO (voltage controlled oscillator) circuit. Certain process parameters should be taken care of while designing of oscillator. With the scaling of transistor size power consumption in the circuit is the main reason for concern for efficient performance of the circuit designed. Having modification in the circuit with techniques SVL have not only enhanced the performance of the circuit but reduced the leakage power in the circuit designed too. By applying leakage reduction techniques in the VCO circuit, efficiency in the circuit has increased with faster speed and lower noise. The circuits are simulated in cadence virtuoso tool at 45 nm technology.

Keywords: VCO, CSVCO, Ring VCO, SVL, Leakage power, leakage current.

I INTRODUCTION

VCO circuit is used in the field of communication system for the generation of the periodic signal. In the digital domain these periodic signal is used for the generation of the timing signals. While in the analog domain it is used as frequency signals. A VCO circuit is a function of voltage and frequency signal. With the change in the applied voltage apparent change in the frequency takes place. Thus VCO circuit for better and efficient performance is the main objective of the designer for designing the circuit in the changing trend of technology. VCO circuit shows linearity when plotted against voltage and frequency. VCO circuit suffers the effect of noise, speed and leakage power in the circuit. So various leakage reduction techniques are being implied the VCO circuit for better output response.

VCO circuit can be designed using various techniques like LC (Inductor-Capacitor) circuit, ring oscillator, Schmitt Trigger etc. For lower power consumption the VCO circuit is designed using the ring oscillator and current starved VCO. Among this other advantages of designing VCO using ring oscillator and CSVCO is that they are easy to design, smaller chip area and have larger signal swing. But while designing the VCO circuit uncertainty jitter should be taken into consideration. In ring oscillator VCO frequency of the circuit is proportional to delay time.

II PROPOSED CIRCUIT

While designing of any circuit, care must be taken in power consumption of the circuit. With the effect of power consumption i.e., static power and dynamic power, speed of the operation is also taken into consideration. Circuit should consume low power and must operate at high speed. SVL leakage reduction techniques are being applied in the circuit for lowering the leakage power in the circuit and for enhancing the performance in the circuit.

Different VCO circuits designed in this paper:

(a) SVL technique in Ring Oscillator VCO
(b) SVL technique in Current starved Oscillator VCO

(a) SVL technique in Ring Oscillator VCO

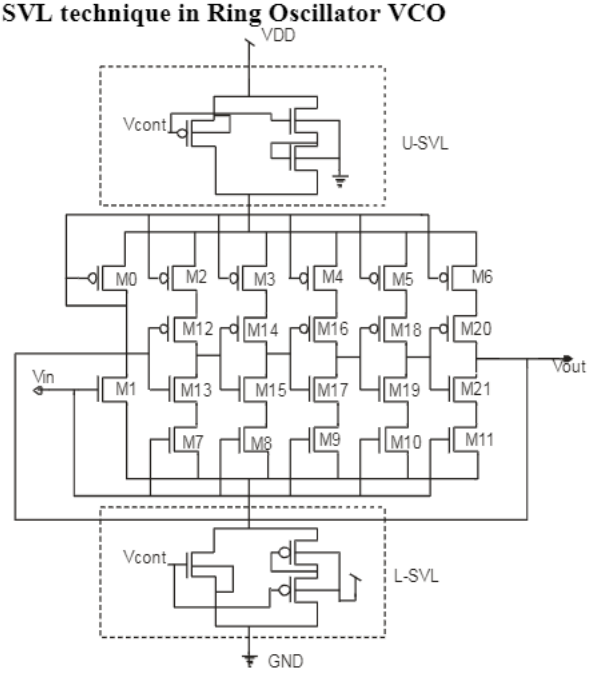

Fig. 1 SVL in VCO Using Ring Oscillator

SVL stands for "Self-controllable voltage level". SVL technique is introduced to overcome the limitations of the MTCMOS technique. It is of two types, L-SVL and U-SVL. It can work separately or both can be introduced in the circuit at the same time. When the oscillator circuit is in active state then Upper Vcont = low (0) and lower Vcont = high (1), then both the sleep transistor in upper and lower part is in ON state. Due to this maximum supply voltage and minimum ground stage voltage is provided to the circuit. Thus the operating speed of the circuit is increased. When the circuit is off then Upper Vcont = high (1) and lower Vcont = low (0). Thus

minimum supply voltage and higher ground level is provided to the circuit. This will effectively decrease the leakage current in the circuit. SVL technique in VCO is shown in Fig1.

(b) SVL technique in Current starved Oscillator VCO

Self voltage level technique is applied on the Current Starved VCO circuit. The SVL circuit commonly consists of a lower SVL circuit and an upper SVL circuit. The lower SVL circuit is formed pull down n-MOSFET switch which is connected in parallel with series connected two p-MOSFET resistors. The pull down n-MOSFET switch and only one of the PMOS resistors are handled by a complement square wave clock (Clk) signal. The upper SVL circuit is formed by a pull up p-MOSFET switch which is joined in parallel with series connected two n-MOSFET resistors. The pull up p-MOSFET switch and n-MOSFET only one resistors are handled by a square wave clock (Clk) signal.

The SVL circuit (lower and upper) is used one by one on the circuit and various circuit parameters were calculated like leakage current, leakage power, noise and power consumption as shown further in simulation results. The circuit has operate in two modes first is the active mode and second is the standby mode. Active mode is the normal operational mode of the load circuit in which the upper and the lower SVL circuit which do one's best to make the load circuit of Current starved VCO act normally to produce its desired functionality. In Standby mode the load circuit avoids its normal operation.

(i) Upper SVL Technique

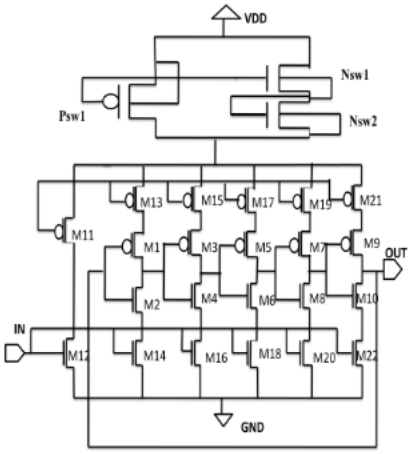

Fig. 2 Circuit Diagram of U-SVL Technique

In the active mode of Figure 2 when the load circuit is active, in this case upper SVL will turn ON p-MOSFET (Psw1) switch and turn OFF both n-MOSFET (Nsw1 and Nsw2) resistors. Thus the ON p-MOSFET switch will connect a direct path connection of the supply voltage Vdd to the load circuit. Hence the circuit operates in standby mode the circuit controlling is low, this low pulse as a complement in upper SVL will turn OFF p-MOSFET switch and turn ON both n-MOSFET resistors and the upper PMOS and NMOS transistor connected in series and supply voltage VDD is applied to the transistor. The gate leakage current maybe decreases in this way.

(ii) Lower SVL Technique

In the active mode of Figure 3 the circuit will turn ON the n-MOSFET (Nsw3) switch and turn OFF both the serially connected Psw2 and Psw3 resistors. Thus ground supply is provided directly by ON n-MOSFET to the circuit for operation. On the other part standby mode as a signal are low then n-MOSFET switch is OFF and both p-MOSFET resistor turn ON connecting a ground supply to the circuit.

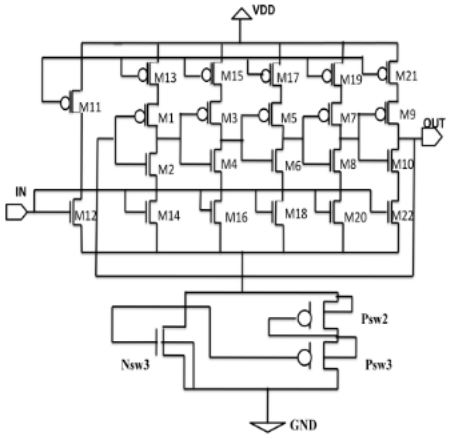

Fig. 3 Circuit Diagram of L-SVL Technique

(iii) Current Starved Voltage Controlled Oscillator Using Combined (LSVL + USVL)

The upper and lower SVL is applied together to the load circuit as shown in Figure 4. To give decreased supply voltage and enhance ground voltage level to the circuit in standby mode of operation and supports normal supply voltage and ground voltage in active mode.

These leakage current waveforms are used for calculating the leakage power and the total dissipated power at respective varying supply voltage.

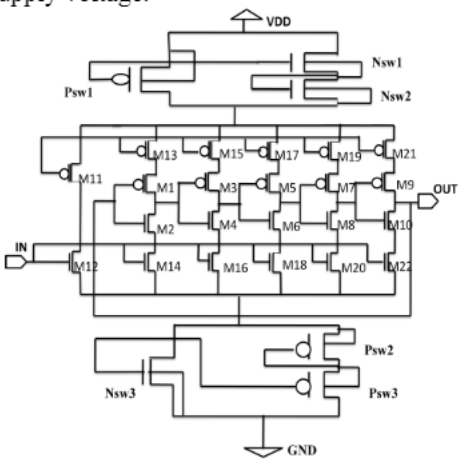

Fig. 4 Circuit Diagram Using Combined (LSVL + USVL) Technique

III SIMULATION RESULT

(a) Leakage Power

The leakage power in the current starved VCO circuit is given as follows in Equation (1)

$$P_{Leakage} = V_{DD} \times \Sigma I_{leakage} \quad (1)$$

$I_{leakage}$ = penetrating leakage current in the turn OFF transistors Leakage power which directly depends upon leakage current from CMOS implemented current starved circuit and SVL (upper and lower SVL) based current starved VCO circuit. Figure 5 reflects graphical analysis of leakage power reduction.

Table 1
Leakage Power in CSVCO

Voltage	Simple Current Starved VCO	U-SVL	L-SVL	Both(L-SVL and U-SVL)
0.7V	12.80nW	9.91nW	6.86nW	0.97nW
0.8V	17.45nW	12.7nW	8.70nW	2.34nW
0.9V	20.90nW	25.09nW	13.02nW	1.67nW
1V	26.01nW	20.95nW	14.89nW	3.99nW

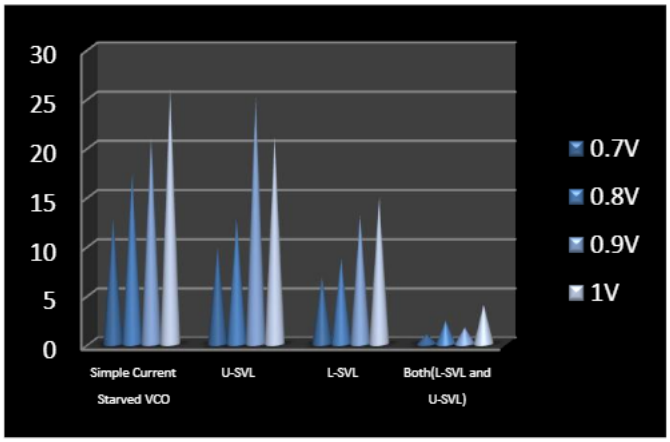

Fig. 5 Graph of Leakage Power in CSVCO

(b) Leakage Current

Leakage current of the current starved VCO is calculated with the help of this equation.

$$I_{leak} = I_{sub\text{-}thr} + I_{gate\text{-}ox} \quad (2)$$

Where, Isub-threshold = sub-threshold leakage current, Igate-ox = gate – oxide leakage current.

Basically leakage current is found in two ways, firstly standby mode and other one is active mode.

Table 2
Leakage Current in CSVCO

Voltage	Simple Current Starved VCO	U-SVL	L-SVL	Both(L-SVL and U-SVL)
0.7V	8.65nA	7.46Na	4.18nA	1.28Pa
0.8V	12.03nA	9.85nA	7.23nA	1.89pA
0.9V	14.98nA	11.53nA	9.12nA	2.99pA
1V	26.99nA	18.21nA	11.22nA	3.59Pa

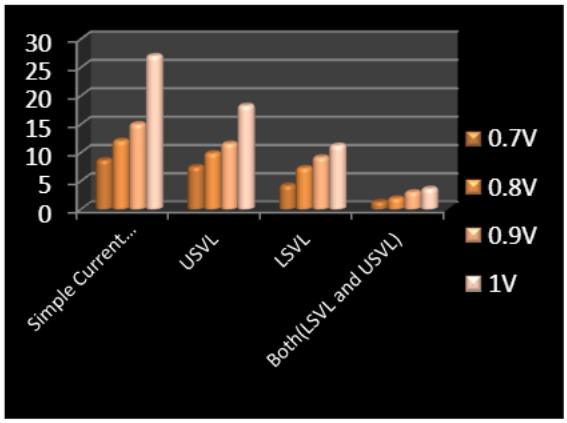

Fig. 6 Graph of Leakage Current in CSVCO

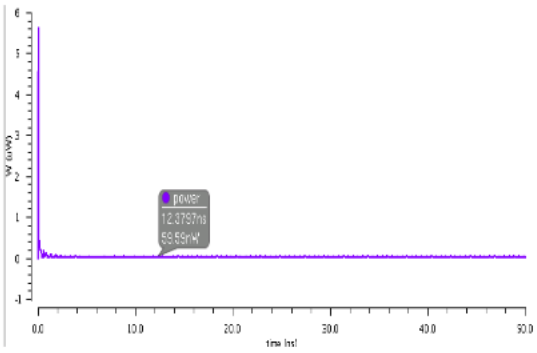

Fig. 7 Leakage power waveform of Current Starved VCO using Combined (LSVL + USVL) Technique

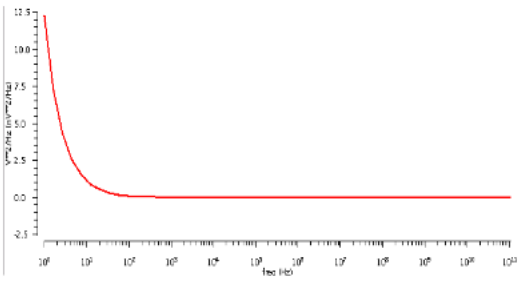

Fig. 8 Noise Waveform of Current Starved VCO Using Combined (U-SVL and L-SVL) Technique

Table 3
of various parameters calculated for the Ring oscillator VCO

Sl. No.	Parameters	SVL in Ring Oscillator VCO
1.	Efficiency (%)	15.76
2.	Voltage Gain (dB)	0.691
3.	Delay (sec)	5.165e-9
4.	Leakage Power (pW)	5.23

IV CONCLUSION

SVL based Current starved VCO circuit is designed and simulated on cadence virtuoso tool at 45nm semiconductor node. In this paper, a new leakage reduction technique is employed to SVL based current starved VCO for performance improvement in terms of leakage, power and noise. The efficiency of the proposed leakage reduction techniques is demonstrated using USVL, LSVL and than combination of both is applied in the circuit. The SVL based current starved circuit also shows a great reduction in terms of circuit noise as the delay reduces to 31 % from the noise analyzed in conventional current starved circuit. In USVL, LSVL and combination of USVL+LSVL based current starved the leakage current observed is 1.89pA at 0.8 volt supply.

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