# Review of CMOS LC Voltage Controlled Oscillators

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**ABSTRACT**
*In this paper, we review CMOS LC Voltage Controlled Oscillators (VCO) for wireless multi-standard transceivers and wireless communications. The main parameters, such as power dissipation, Tuning range, phase noise, carrier frequency, supply voltage figure of merit (FOMt) were reviewed.*

***Keywords***—*CMOS, LC VCO,microelectronics, Nanoelectronics.*

## I INTRODUCTION

In recent years wireless communication market was still growing. Such situation increased the demand for low cost integrated transceivers. Because communication standards are becoming more complicated, requirements for such transceiver parameters as noise, linearity and power consumption are at the limits of technology. This forces RF IC designers to explore design trade-offs very deeply for each circuit, which makes design process much longer. This at the end has an impact on transceivers price. To help the designer, aiding tools should be created in order to make the design process easier and faster. Transceiver is the main part of the wireless system and its main function is to receive and transmit data. The basic transceiver consists of the following blocks: low noise amplifier (LNA), power amplifier (PA), down-conversion mixer, up-conversion mixer, filters and frequency synthesizer. In transceivers the phase locked loop (PLL) is mainly used as the frequency synthesizer.

A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL is capable of tracking the phase changes that falls in this bandwidth of the PLL. A PLL also multiplies a low-frequency reference clock $CK_{ref}$ to produce a high-frequency clock $CK_{out}$ this is known as clock synthesis.
A PLL has a negative feedback control system circuit. The main objective of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is achieved after many iterations of comparison of the reference and feedback signals. In this lock mode the phase of the reference and feedback signal is zero. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant.

The basic block diagram of the PLL is shown in the Figure 1. In general a PLL consists of five main blocks:
(a) Phase Detector or Phase Frequency Detector (PD or PFD)
(b) Charge Pump (CP)
(c) Low Pass Filter (LPF)
(d) Voltage Controlled Oscillator (VCO)
(e) Divide by N Counter

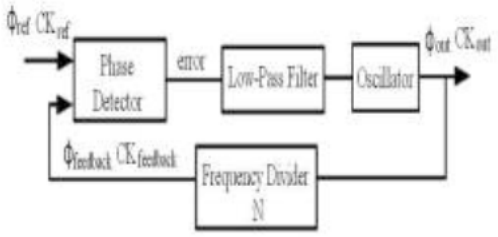


**Fig. 1 Basic block diagram o a PLL**

Commonly two types of VCOs: ring oscillators (Ring-VCOs) and LC oscillators (LC-VCOs) are used in high-frequency PLL. The Ring-VCOs take a small area on a chip and can provide very wide tuning range but their phase noise performance is very poor when compared to LC-VCOs. LC-VCOs can operate in high frequency, but their tuning range is relatively small and on-chip inductors occupy a lot of chip area.

The schematic of basic LC-VCO is shown in Fig. 2. The LC-VCO consists of the following parts: high-quality inductor (L), varactors block, switched capacitors block, cross-coupled transistors (M1, M2) and current control block. The inductor with varactors and the switched capacitors block form a LC tank. The negative resistance of the LC-VCO is given by the transconductance of the cross coupled M1 and M2 NMOS or PMOS transistors. They generate the negative resistance to cancel the loss in the LC tank so that the circuit can enable sustained oscillation.

**(a) Switched Capacitor Block-** First, confirm that you have the correct template for your Frequency calibration is consisted by two steps of fine tuning and coarse tuning to widen the operating frequency range. The coarse tuning is obtained using the switched capacitor block. A switched capacitor block is used in classic design. The block consists of capacitors arrays connected in parallel, which can be turned on or off depending on the required capacity. When the blocks are switched on, the capacity is reduced, when the blocks are switched off, the capacity increases. Switches in the LC-VCOs is realized using NMOS or PMOS transistors or capacitors.

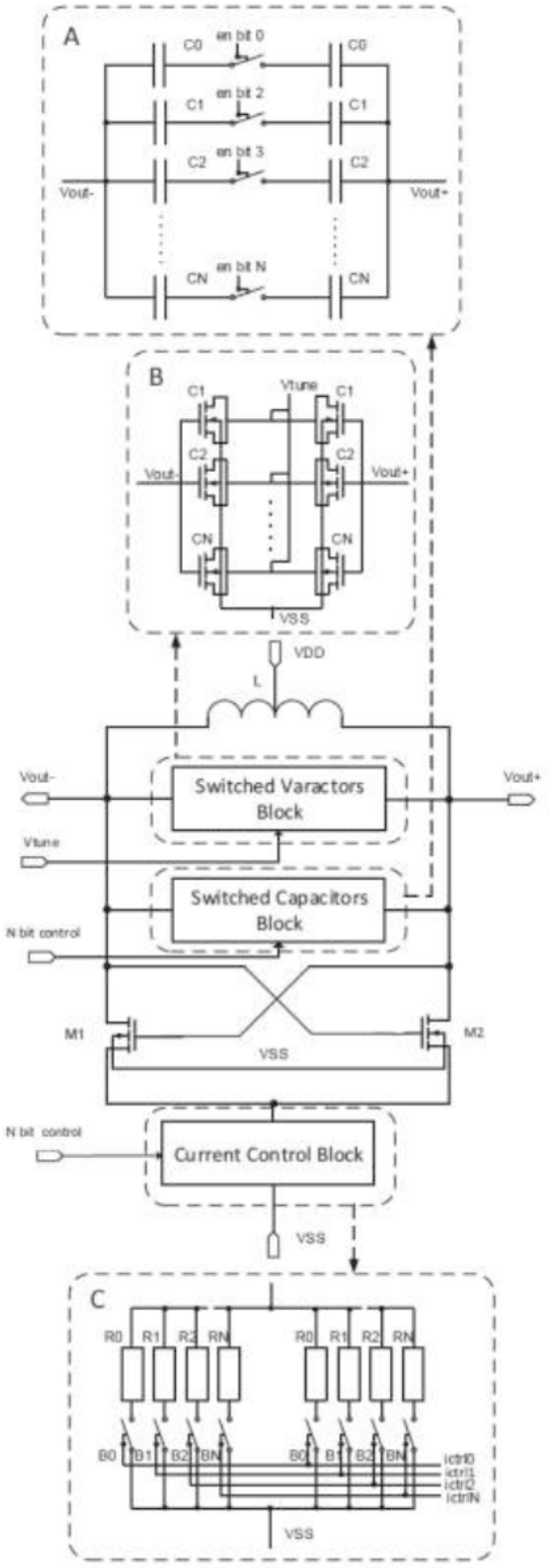


**Fig. 2. Schematic of basic LC-VCO.**

**(b) Varactor Block-** The fine tuning is obtained using the varactors block in order to get precise operation frequency. This block consists of parallel connected multi-fingered varactors. These varactors maximize the tunability of the LC-VCOs. The external voltage $V_{tune}$ is used for varying linearly the equivalent capacitance of varactors. Basically $V_{tune}$ control voltage can range from 0 V to ~5 V.

**(c) Current Control Block-**The last component of the LC-VCO is the current control block. In this block bias current is controlled by several bits. As can be seen in Fig. 2, ictrl is a binary array of several independent control signals for corresponding bias current switches. Therefore, by choosing ictrl signals, the LC-VCO can get various bias current values, which means that LC-VCO can adjust its power consumption to the optimum. Compared with bandgaps reference current biasing this structure has the advantage of simplicity and power consumption selection flexibility [2-4].

The paper is organized as follows: section II describes the analysis of the LC-VCOs overview; conclusions are summarized in section III.

## II LC VCOS OVERVIEW

This paper provides an overview of thirty five different VCOs. All information has been compiled from IEEE Xplore digital library. The results comparison of VCOs are given in Table I and Table II . The main parameters of the VCO are: IC technology ***Tch.*** (nm)- carrier frequency ***Fc*** (GHz), frequency tuning range **F** (%), phase noise ***PN*** (dBc/Hz), power dissipation ***P*** (mW), figure of merit ***FOMt*** (dBc/Hz).

**Table 1**
**Performance Comparison of VCOS (Micro)**

| Nr. | Tch., nm | Fc, GHz | F, % | PN, dBc/Hz | PN@f, MHz | P, mW | FOMt, dBc/Hz |
|---|---|---|---|---|---|---|---|
| [5] | 350 | 5.88 | 3.91 | -112 | 1 | 19.2 | -166.4 |
| [6] | 250 | 7.45 | 30.76 | -100 | 1 | 0.54 | -189.9 |
| [7] | 250 | 4.89 | 13.69 | -124 | 1 | 22 | -186.7 |
| [8] | 250 | 3.61 | 6.38 | -130.7 | 1 | 22.6 | -184.4 |
| [9] | 180 | 4 | 47.7 | -115.6 | 1 | 2.99 | -196.5 |
| [10] | 180 | 12.77 | 15.75 | -110.2 | 1 | 1.08 | -195.9 |
| [11] | 180 | 1.85 | 9.21 | -126 | 1 | 1.35 | -189.3 |
| [12] | 180 | 13 | 25.62 | -101.4 | 1 | 2.4 | -188.1 |
| [13] | 180 | 18.9 | 1.06 | -129.3 | 1 | 10 | -185.3 |
| [14] | 180 | 1.82 | 10.99 | -127 | 1 | 6.3 | -185 |
| [15] | 180 | 5.52 | 7.52 | -122 | 1 | 13.5 | -182.7 |
| [16] | 180 | 5.36 | 13.81 | 127 | 3 | 18 | -182.3 |
| [17] | 180 | 12.31 | 28.11 | -108 | 0.1 | 50 | -180.9 |
| [18] | 180 | 3.5 | 21.21 | -91 | 1 | 5.04 | -181.8 |
| [19] | 180 | 5.56 | 15.5 | -105.8 | 1 | 3.6 | -176.9 |
| [20] | 180 | 7.65 | 6.54 | -108.3 | 1 | 4.9 | -175.4 |
| [21] | 180 | 29.82 | 1.38 | -104.1 | 1 | 2.3 | -172.7 |
| [22] | 180 | 5.25 | 0.76 | -117.8 | 1 | 1.05 | -169.5 |
| [23] | 180 | 2.05 | 53.08 | -83.82 | 1 | 11.2 | -155.5 |
| [24] | 130 | 5.71 | 37.69 | -132.7 | 1 | 2.21 | -215.9 |
| [25] | 130 | 3.88 | 37.42 | -138 | 3 | 13.6 | -200.4 |
| [26] | 130 | 13.93 | 13.29 | -100.5 | 1 | 0.6 | -188.2 |
| [27] | 130 | 4.9 | 2.5 | -135.7 | 3 | 3 | -183.2 |
| [28] | 130 | 8.58 | 15.51 | -106.2 | 1 | 4 | -182.7 |
| [29] | 130 | 13.75 | 10.91 | -104.5 | 1 | 5 | -181.1 |
| [30] | 130 | 19.48 | 4.88 | -103 | 1 | 5 | -175.6 |
| [31] | 130 | 6 | 5.33 | -115 | 1 | 12.5 | -174.1 |

**Table 2**
**Performance Comparison of VCOS (Nano)**

| Nr. | Tch., nm | Fc, GHz | F, % | PN, dBc/Hz | PN@df, MHz | P, mW | FOMt, dBc/Hz |
|---|---|---|---|---|---|---|---|
| [32] | 90 | 34.34 | 62.12 | -100.80 | 1 | 20.00 | -194.37 |
| [33] | 90 | 5.63 | 45.12 | -108.00 | 1 | 14.00 | -184.64 |
| [34] | 90 | 15.06 | 5.84 | -94.86 | 1 | 13.69 | -162.39 |
| [35] | 65 | 1.17 | 83.44 | -124.30 | 1 | 2.40 | -200.28 |
| [36] | 65 | 3.54 | 34.46 | -142.10 | 10 | 13.70 | -192.46 |
| [37] | 65 | 4.50 | 77.78 | -110.00 | 1 | 9.36 | -191.17 |
| [38] | 65 | 6.85 | 27.74 | -118.30 | 1 | 20.20 | -190.82 |
| [39] | 65 | 6.85 | 27.74 | -118.30 | 1 | 20.20 | -190.82 |

The main parameters was separated into **micro** (Table I) and **nano** (Table II) sections in order to view the information more obviously. VCOs designed in 350–130 nm IC technology belongs in **micro** section, and VCOs designed by 90–65 nm belongs in **nano** section.

To evaluate the overall performance of the VCO, a figure-of-merit including the tuning range ($FOM_T$) is used.

$$FOM_T = PN(\Delta f) - 20\log(F_c/\Delta F) + 20\log(\Delta f/10) + 10\log(P/1mW) \quad \ldots\ldots(1)$$

where $PN(\Delta f)$ is the phase noise at an offset frequency $f$, $Fc$ is the carrier frequency, $P$ is the power consumption in mW and $F$ is a percentage of the frequency tuning range. In this paper all VCOs $FOM_T$ values was recalculated by formula (1) and shown in Table I and Table II.

In micro technology,the lowest $FOM_T$ is in 24th VCO ($FOM_T$ = –215.88 dBc/Hz). This VCO is designed in 0.13µm IC technology.

In nano technology,The lowest $FOM_T$ is in 35th VCO ($FOM_T$ = –200.28 dBc/Hz). This VCO is designed in 65nm IC technology.

## III CONCLUSION

This paper provides an overview and analysis of forty (in Table I and Table II [5]–[44]) different VCOs. Overview was separated into **micro** and **nano** sections in order to view the information more obviously. VCOs designed in 0.35 – 0.13 µm IC technology belongs **micro** section, and VCOs designed in 90 – 65 nm belongs **nano** section. The folowing parameters were taken into account during this analysis: IC technology **Tch.** (nm), carrier frequency **Fc** (GHz), frequency tuning range **F** (%), phase noise **PN** (dBc/Hz), power dissipation **P** (mW) and figure of merit **FOMt** (dBc/Hz).

The lowest *FOMT* in **micro** section is in 24th VCO (*FOMT* = –215.88 dBc/Hz). This result was affected by following parameters: very low phase noise at 1 MHz offset from carrier frequency (*PN* = –132.68 dBc/Hz), low power consumption (*P* = 2.21 mW) and wide frequency tuning range (*ΔF*= 37.69 %). This VCO was designed in 0.13 µm IC technology.
The lowest *FOMT* in **nano** section is in 35th VCO (*FOMT* = –200.28 dBc/Hz). This result was affected by following parameters: low phase noise at 1 MHz offset from carrier frequency (*PN* = –124.30 dBc/Hz), low power consumption (*P* = 2.4 mW). This VCO was designed in 65 nm IC technology.

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