Review of Hardware on Fractal Image Compression

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ABSTRACT
Fractal Image Compression is a promising compression technique in terms of its high compression ratios and fidelity. It has fast decoding, independent resolution and good image quality at low bit-rates which is useful for offline applications. Large encoding time has limited the use of this compression technique. In fractal based image encoding an image is divided into sub-blocks and the root mean square metrics among them are calculated. To reduce the encoding time various hardware are being implemented. In this paper we are studying most significant hardware implementations in Fractal Image Compression. The hardware design are aimed at substantially speeding up the encoding process by performing many of the repetitive tasks involved in finding transformations in parallel.

Index Terms—Hardware, Image, Pixel

I INTRODUCTION

The basic idea of fractal compression is to search the similarities between larger and smaller portions of an image by partitioning the original image into blocks of fixed size, called range and creating a shape codebook from the original image of double size of the range, called domain. Range blocks partition the image so that every pixel is included while the domain blocks can be overlapped and/or to not contain every pixel. The number of pixels remains unchanged even while extrapolating the image. Fractal image compression algorithms represent an image as a series of contractive transformations, each of which maps a large domain block to a smaller range block. Given only this set of transformations, it is possible to reconstruct an approximation of the original image by iteratively applying the transformations to an arbitrary image. Different hardware implementation are done in Fractal image compression to reduce the large number of comparisons yielding a substantial speed up and make it more flexible to make it applicable for different applications.

II HARDWARE IMPLEMENTATION IN FRACTAL IMAGE COMPRESSION

(a) Fractal Compression implemented with SIMD (Single Instruction Multiple Data)- Xue, M., Hanson, T., Merigot (1994) used a pixel-based parallelization scheme on a pyramidal SIMD architecture for a non-adaptive version of fractal compression.

Giordano, S., Pagano, M., Russo, F., Sparano, D.: (1996) gave a multi-scale fractal image coding algorithm based on SIMD parallel hardware [4]. An image-block parallelization scheme is used on a SIMD array processor.

Palazzari, P., Coli, M., Lulli, G (1999) massively parallel processing approach has been used on an APE100/Quadrics SIMD machine. For testing, 512 floating point processors has been used, offering a peak power of 25.6 GFLOPS. A gray level image of 512x512 has been compressed using a scalar quantization technique in about 2 seconds.

(b) Fractal Compression implemented with GPU (Graphics Processing Unit)- William A.Stapleton,Wagdy Mahmoud and David Jeff Jackson (1996) enhanced the computational speed through an parallel super computer implementation of the fractal image compression on a SIMD parallel machine the nCube-2. The fractal image compression process exhibits algorithmic modification employing a quad tree recomposition approach. The fractal iterated function system (IFS) calculations exhibit a high natural parallelism.

Tai-Chi Lee, Patrick Robinson, Michael Gubody and Erik Henne in (1999). A specialized hardware/software co-processor to improve the performance of encoding/decoding of images using fractal techniques can be used to increase the speed of data compression. A specialized processor is developed using a combination of VHDL logic synthesis, FPGA (Field Programmable Gate Array) hardware, and the C programming language to create a re-configurable hardware co-processor solution that can be adapted to the fractal compression algorithm.

Hidehisa Nagano, Akihiro Matsuura, and Akira Nagoya proposed a method of implementing Fractal Image Compression on dynamically reconfigurable architecture.

Processing Elements (PEs) configured for each image block perform these computations in a pipeline manner. By configuring PEs these computations and the number of address are reduced by half even in the worst case. This reduction increases the number of PEs that work in parallel. In addition, dynamic re-configurability of hardware is employed to omit useless metric computations. Experimental results show that the resources for implementing the PEs are reduced to 60 to70% and the omission of useless metric computations reduces the encoding time to10 to55%.

Ugo Erra presented a parallel fractal image compression using the programmable graphics hardware. It exploits SIMD architecture and inherent parallelism of graphic boards to speed-up baseline approach of fractal encoding. The results are achieved on cheap and available graphics boards. It uses the GPU for image compression. uses the GPU for image compression. Using programmable capabilities of the GPUs the large amount of inherent parallelism and memory bandwidth to perform fast pairing search between portions of the image is exploited. GPUs are an effective co-processors for fractal image processor. For the text image of 256 x 256 pixels range size of 4 x 4 and domain is of 8 x 8 pixels GPU takes about 1 sec while the CPU version takes about 280seconds to perform all pairing. The amount of paring test that the GPU is capable to perform is about 21 millions per second, the CPU performs about 220 thousands paring test per second. Ugo Erra work shows its advantages when compared with expensive parallel architecture as for instance in [3] which use 512 floating-point processors with performance comparable to this GPU implementation

Munesh Singh Chauhan and Ashish Negi (2012) presented a new approach for fractal image compression [1]. They modified and supported with advanced parallel hardware in the form of Graphical Processor Units. The GPUs consist of many cores thus providing SIMD parallel processing capability at an un-imaginable rate of around 24 GFLOPS. This processing speed was not possible earlier before the advent of GPUs except in some selected highly evolved Super computers. The rendering of image and its compression is implemented using OpenCL library. The benefits of faster fractal compression lie in the realm of medical imaging, satellite reconnaissance, gaming & film media.GPU time is considerably lower than CPU timing.

GPU can be used for parallel applications that require intensive computation and have complex algorithmic structures. The graphical units have revolutionized the way scientific computations are done and provide an inexpensive alternative for everyday commodity computing. GPUs have a more affordable avenue for desktop computing. It can also be used in finding self-similarities using IFS in sound waves akin to fractals. The only change being to replace contrast & brightness variables in fractals to that of Fourier transforms for sound waves. Another aspect that is being researched using GPU is the pattern recognition in gene encodings. The Encoding time using GPU clearly shows that it is possible to use fractals for resolution independent video capture format. In an ideal high definition (HD) television, the frame rate required for high fidelity display is 16.67 millisec. Using this rate the content can be rendered on any type of display panel that supports the experiment clearly shows the frame rate below 9 milliseconds which is extremely ideal.

Munesh Singh Chauhan, Sharmi S and Abeer Marhoon Al-Sideiri (2013) did on-board Implementation of Fractal Compression of Satellite Images using Distributed Networked GPUs. Satellite imageries are treated as fractals and then encoding them provides an efficient way of conserving bandwidth and per-bit storage costs.

III CONCLUSION

Fractal image compression using hardware implementation uses inherent parallelism and speeds up the process. It has a great scope in future. Other fast fractal image compression methods can be implemented further on hardware which will increase its speed up more effectively.

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